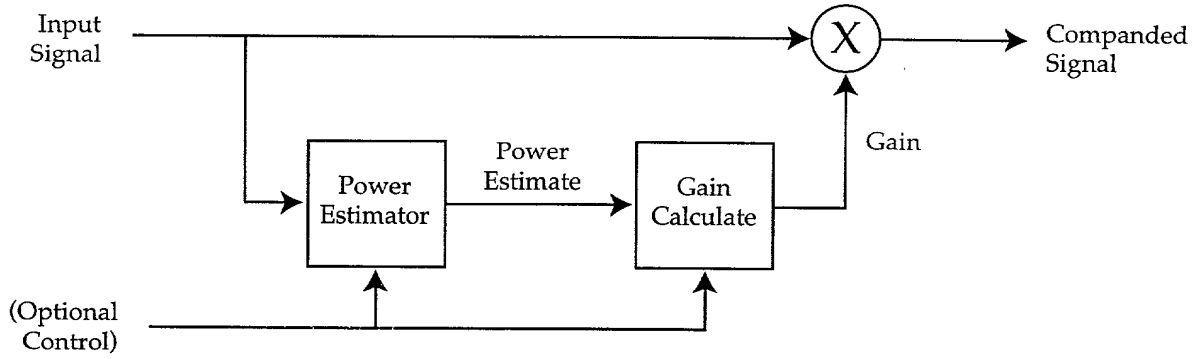


FIG. 1A

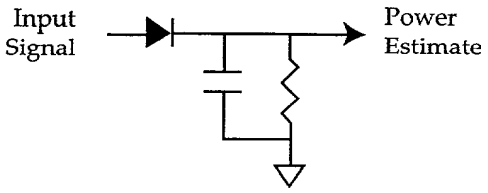


FIG. 1B

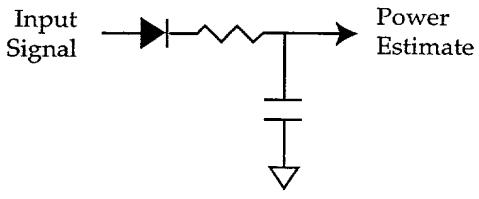


FIG. 1C

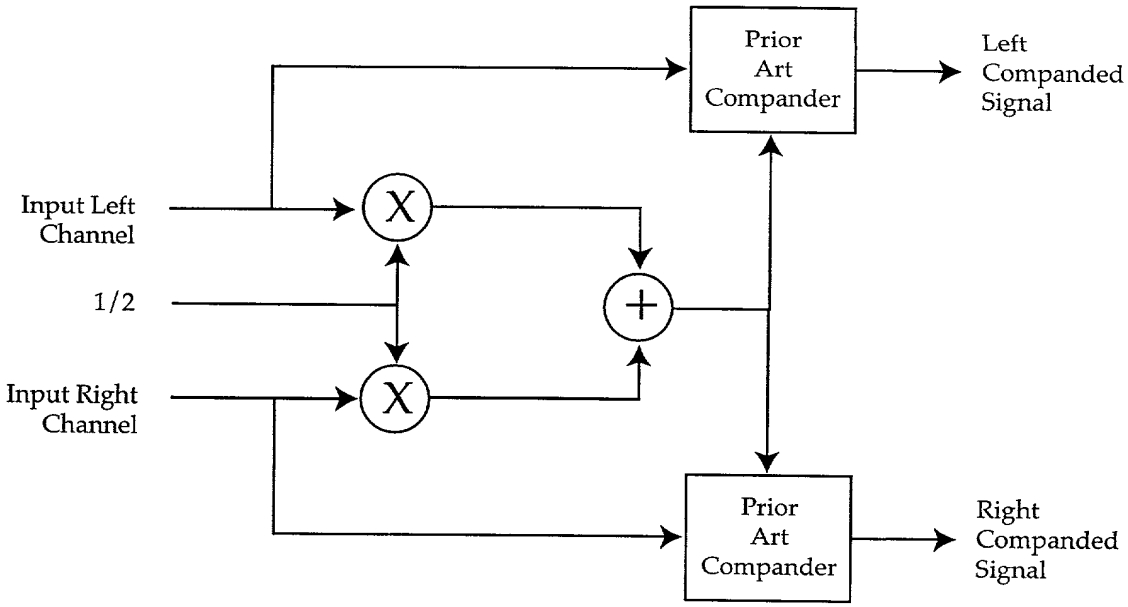

Prior
Art
Compander
Left
Companded
Signal
Input Left
Channel
X
1/2
+
Input Right
Channel
X
Prior
Art
Compander
Right
Companded
Signal

FIG. 1D

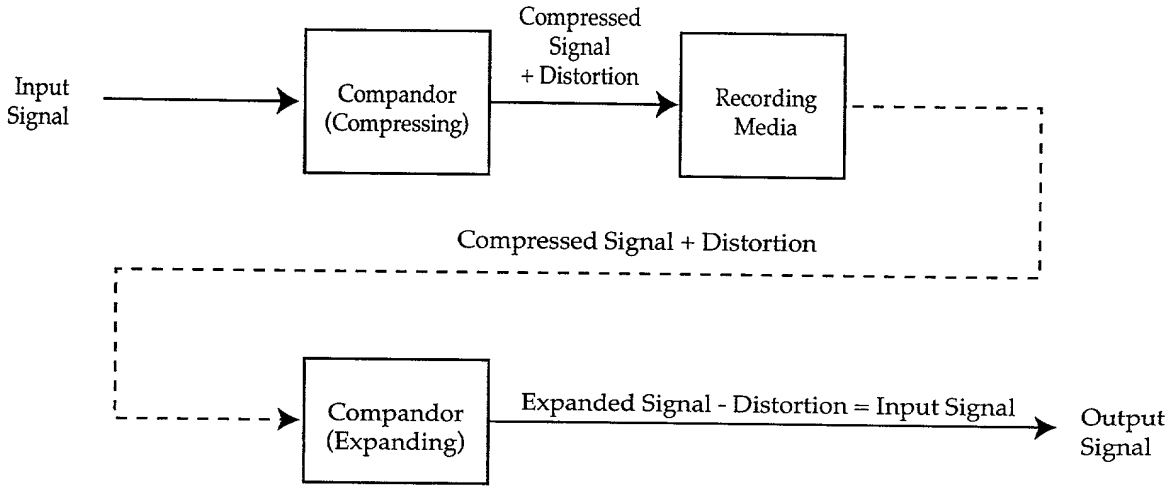

Input
Signal
Compandor
(Compressing)
Compressed
Signal
+ Distortion
Recording
Media
Compressed Signal + Distortion
Compandor
(Expanding)
Expanded Signal - Distortion = Input Signal
Output
Signal

FIG. 1E

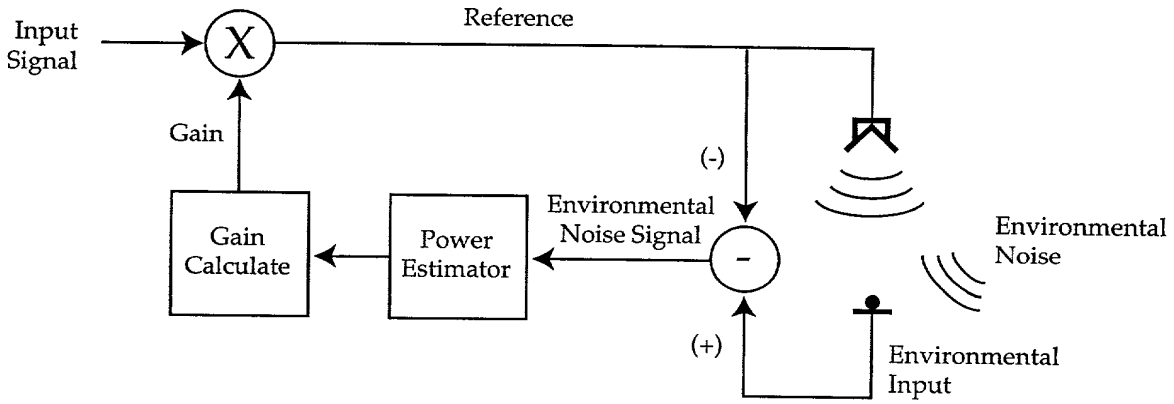

Input
Signal
X
Reference
Gain
(-)
Gain
Calculate
Power
Estimator
Environmental
Noise Signal
-
Environmental
Noise
(+)
Environmental
Input

FIG. 2

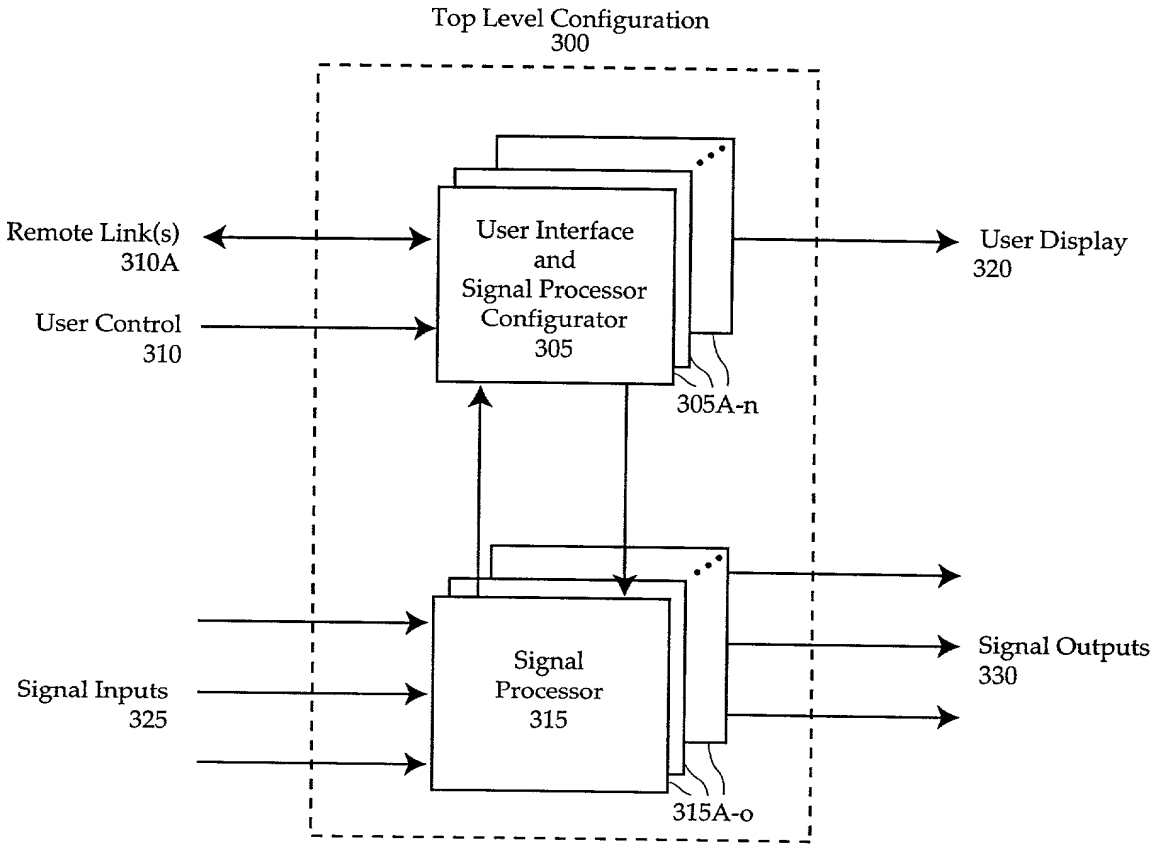

Top Level Configuration
300
Remote Link(s)
310A
User Control
310
User Interface
and
Signal Processor
Configurator
305
305A-n
User Display
320
Signal Inputs
325
Signal
Processor
315
315A-o
Signal Outputs
330

FIG. 3A

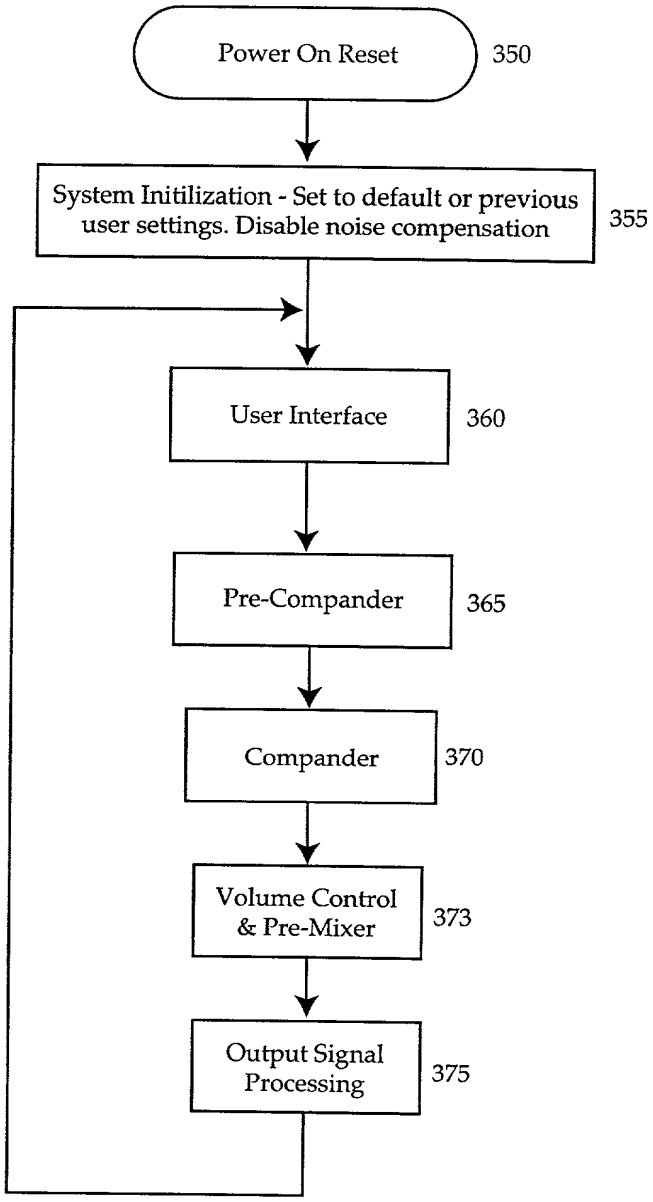

Power On Reset
350
System Initilization - Set to default or previous user settings. Disable noise compensation
355
User Interface
360
Pre-Compander
365
Compander
370
Volume Control & Pre-Mixer
373
Output Signal Processing
375

FIG. 3B

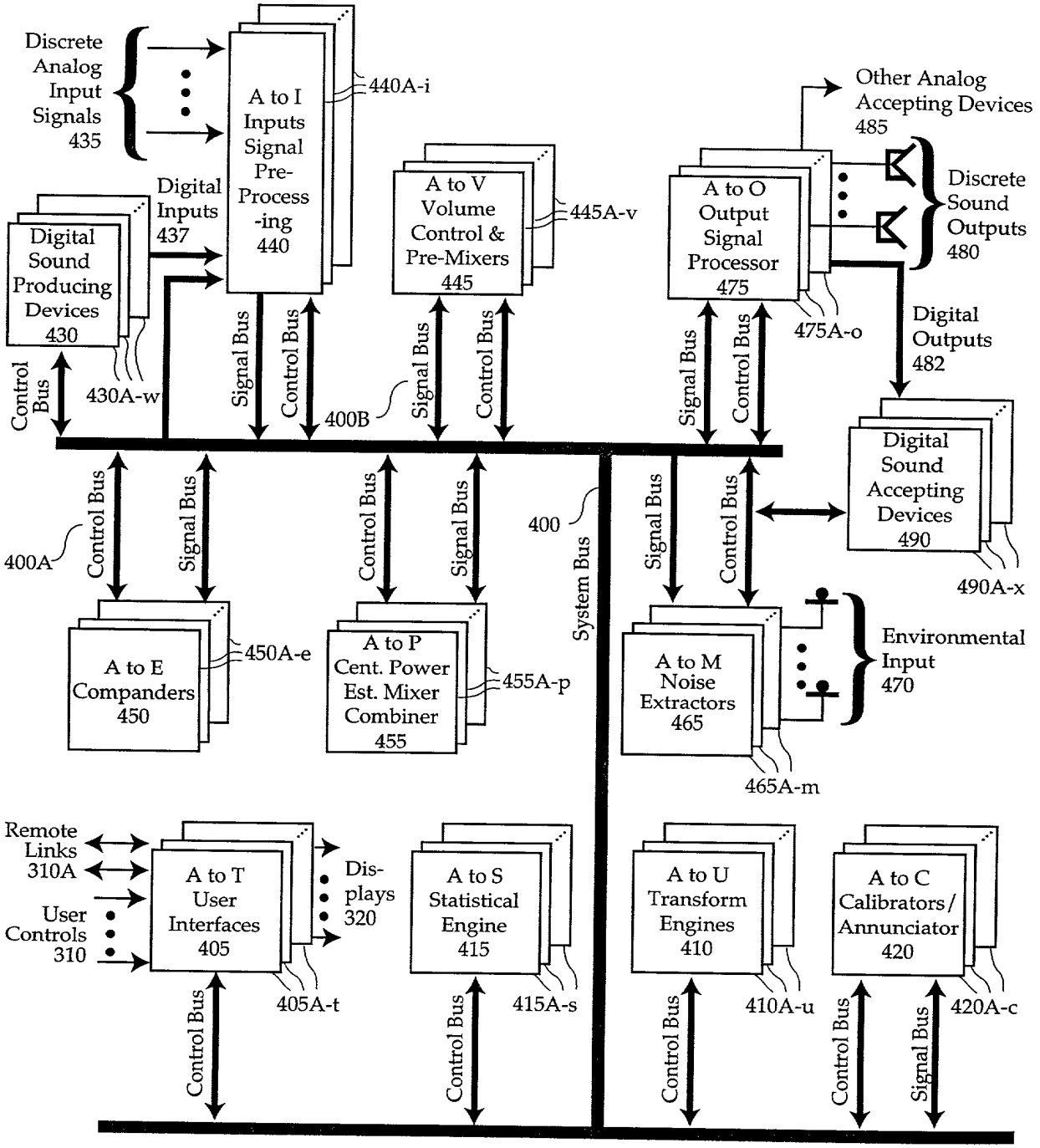

Discrete Analog Input Signals 435
A to I Inputs Signal Pre-Process-ing 440
440A-i
Digital Inputs 437
Digital Sound Producing Devices 430
430A-w
Control Bus
Signal Bus
Control Bus
400B
A to V Volume Control & Pre-Mixers 445
445A-v
Signal Bus
Control Bus
Other Analog Accepting Devices 485
A to O Output Signal Processor 475
475A-o
Discrete Sound Outputs 480
Digital Outputs 482
Signal Bus
Control Bus
Digital Sound Accepting Devices 490
490A-x
400
400A
Control Bus
Signal Bus
A to E Companders 450
450A-e
Control Bus
Signal Bus
A to P Cent. Power Est. Mixer Combiner 455
455A-p
System Bus
Signal Bus
Control Bus
A to M Noise Extractors 465
465A-m
Environmental Input 470
Remote Links 310A
User Controls 310
A to T User Interfaces 405
405A-t
Dis-plays 320
Control Bus
A to S Statistical Engine 415
415A-s
Control Bus
A to U Transform Engines 410
410A-u
Control Bus
A to C Calibrators / Annunciator 420
420A-c
Control Bus
Signal Bus

FIG. 4

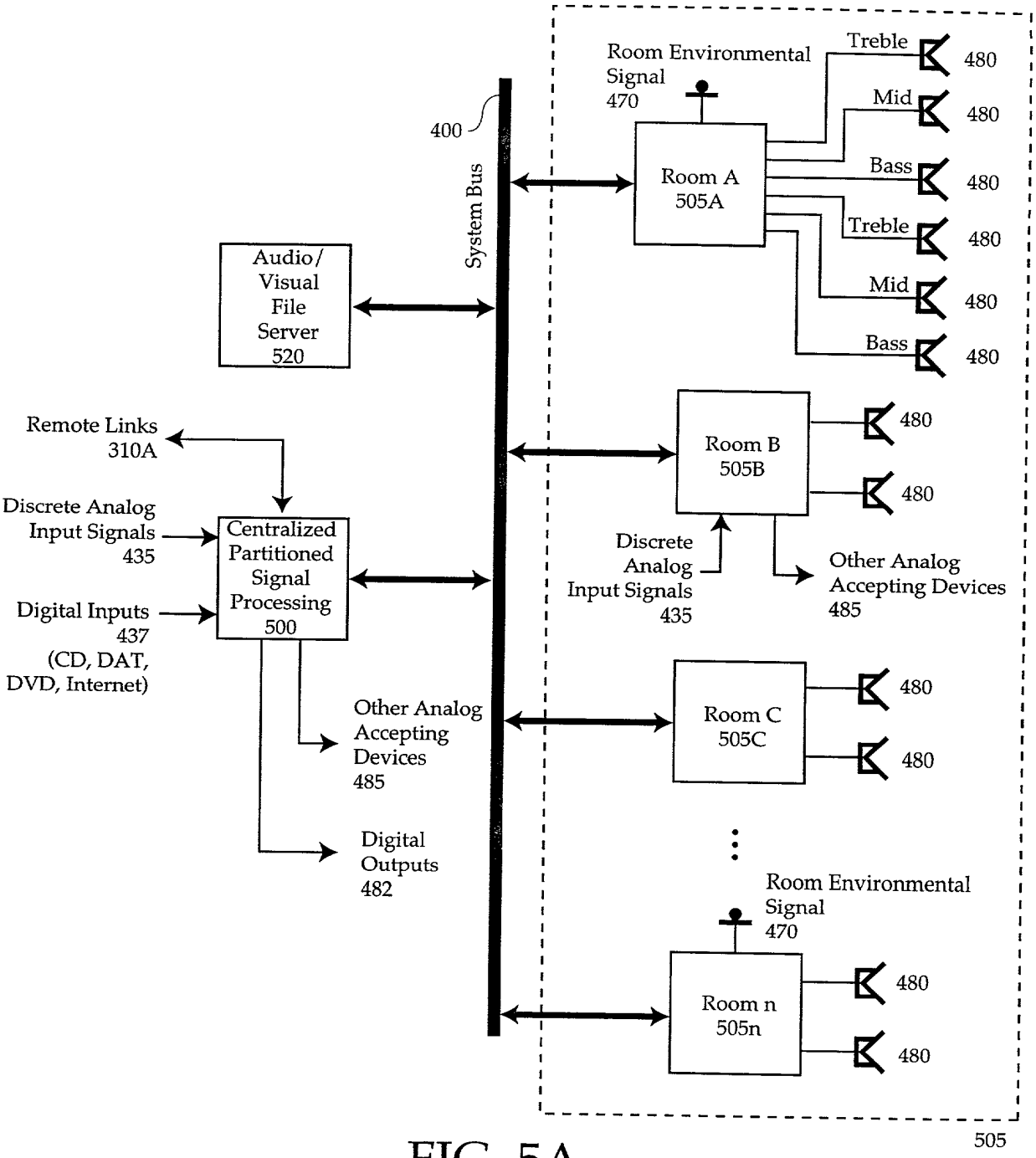

400
System Bus
Audio/
Visual
File
Server
520
Remote Links
310A
Discrete Analog
Input Signals
435
Digital Inputs
437
(CD, DAT,
DVD, Internet)
Centralized
Partitioned
Signal
Processing
500
Other Analog
Accepting
Devices
485
Digital
Outputs
482
Room Environmental
Signal
470
Room A
505A
Treble
Mid
Bass
Treble
Mid
Bass
480
Room B
505B
Discrete
Analog
Input Signals
435
Other Analog
Accepting Devices
485
Room C
505C
Room Environmental
Signal
470
Room n
505n
505

FIG. 5A

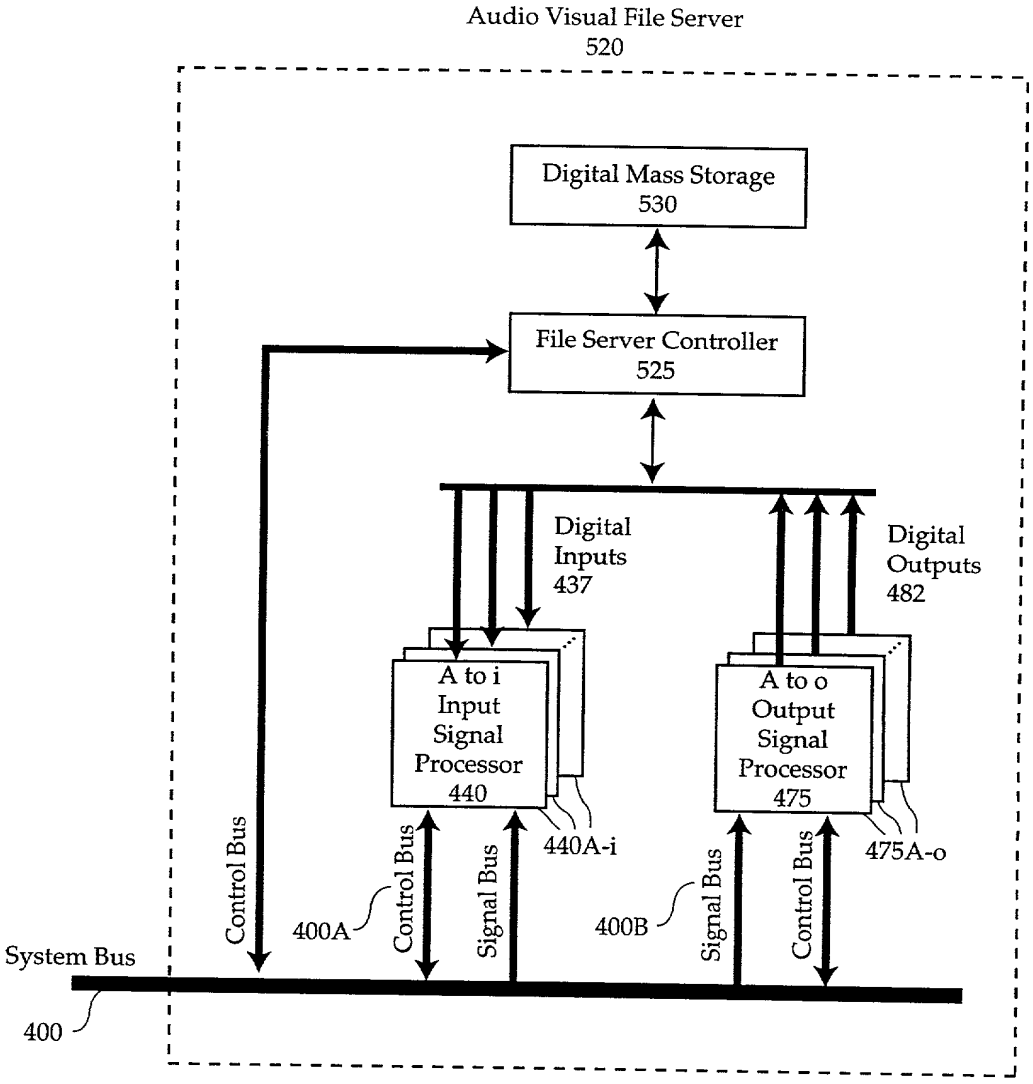

Audio Visual File Server
520
Digital Mass Storage
530
File Server Controller
525
Digital
Inputs
437
Digital
Outputs
482
A to i
Input
Signal
Processor
440
A to o
Output
Signal
Processor
475
440A-i
475A-o
Control Bus
400A
Control Bus
Signal Bus
400B
Signal Bus
Control Bus
System Bus
400

FIG. 5B

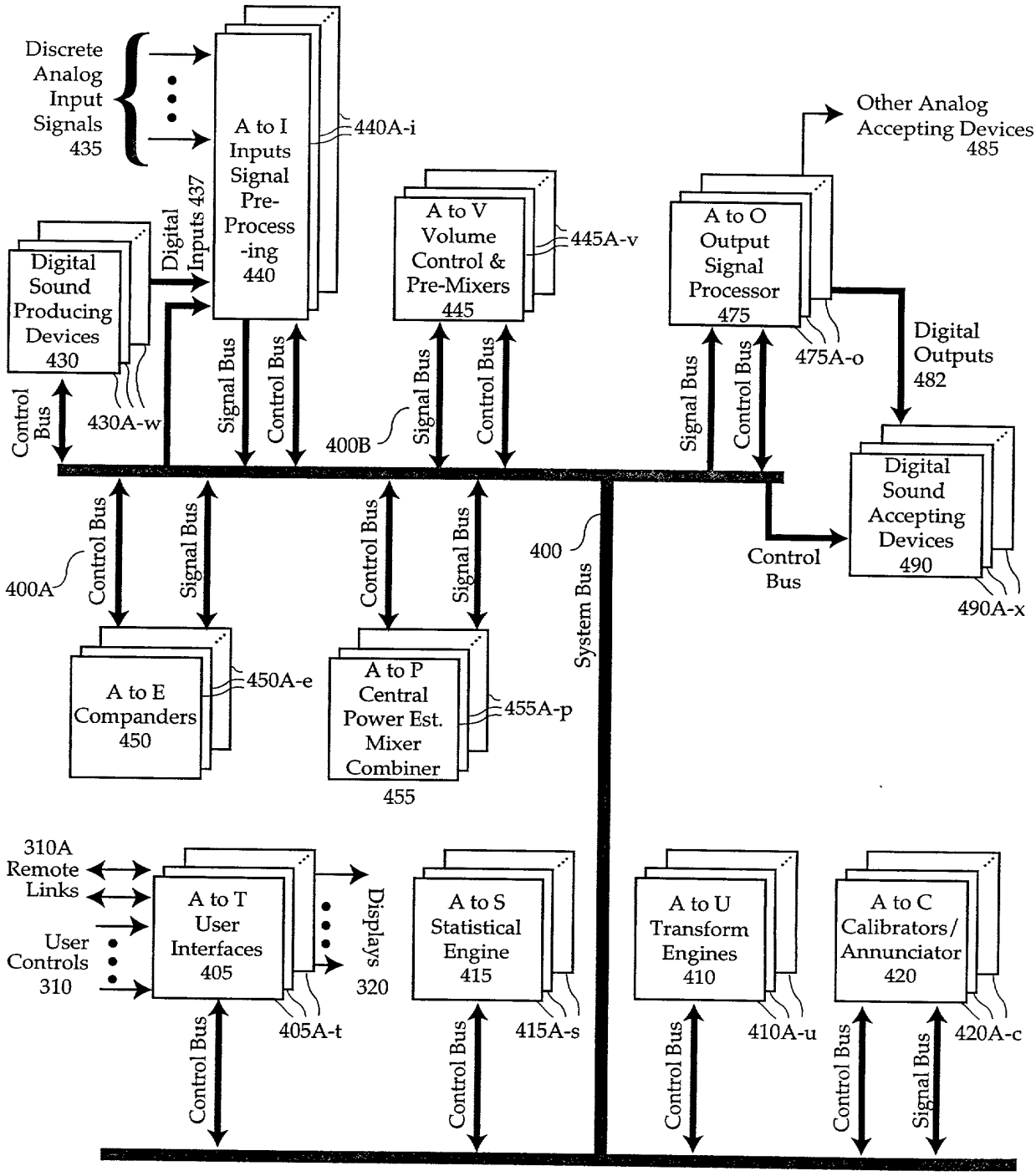

Discrete Analog Input Signals 435
A to I Inputs Signal Pre-Process -ing 440
440A-i
Digital Inputs 437
Digital Sound Producing Devices 430
430A-w
Control Bus
Signal Bus
Control Bus
A to V Volume Control & Pre-Mixers 445
445A-v
400B
Signal Bus
Control Bus
A to O Output Signal Processor 475
475A-o
Other Analog Accepting Devices 485
Digital Outputs 482
Signal Bus
Control Bus
Digital Sound Accepting Devices 490
490A-x
Control Bus
400
System Bus
400A
Control Bus
Signal Bus
A to E Companders 450
450A-e
Control Bus
Signal Bus
A to P Central Power Est. Mixer Combiner 455
455A-p
310A Remote Links
User Controls 310
A to T User Interfaces 405
405A-t
Displays 320
Control Bus
A to S Statistical Engine 415
415A-s
Control Bus
A to U Transform Engines 410
410A-u
Control Bus
A to C Calibrators/ Annunciator 420
420A-c
Control Bus
Signal Bus

FIG. 5C

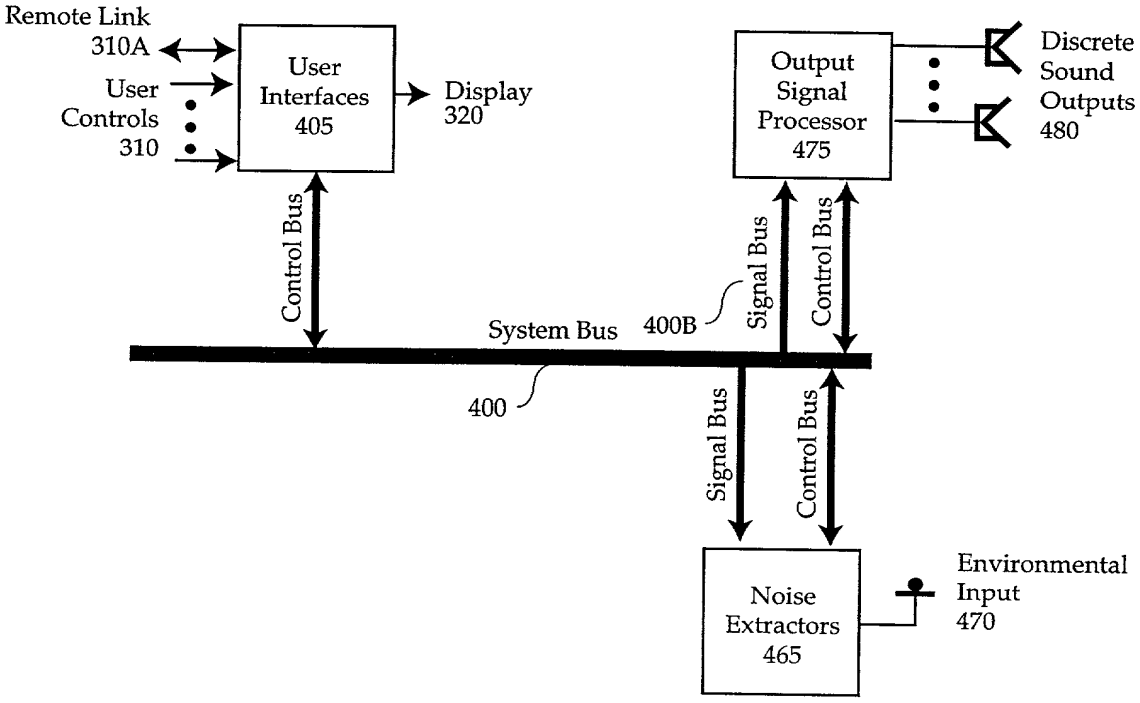

Remote Link
310A
User
Controls
310
User
Interfaces
405
Display
320
Output
Signal
Processor
475
Discrete
Sound
Outputs
480
Control Bus
System Bus
400B
Signal Bus
Control Bus
400
Signal Bus
Control Bus
Noise
Extractors
465
Environmental
Input
470

FIG. 5D

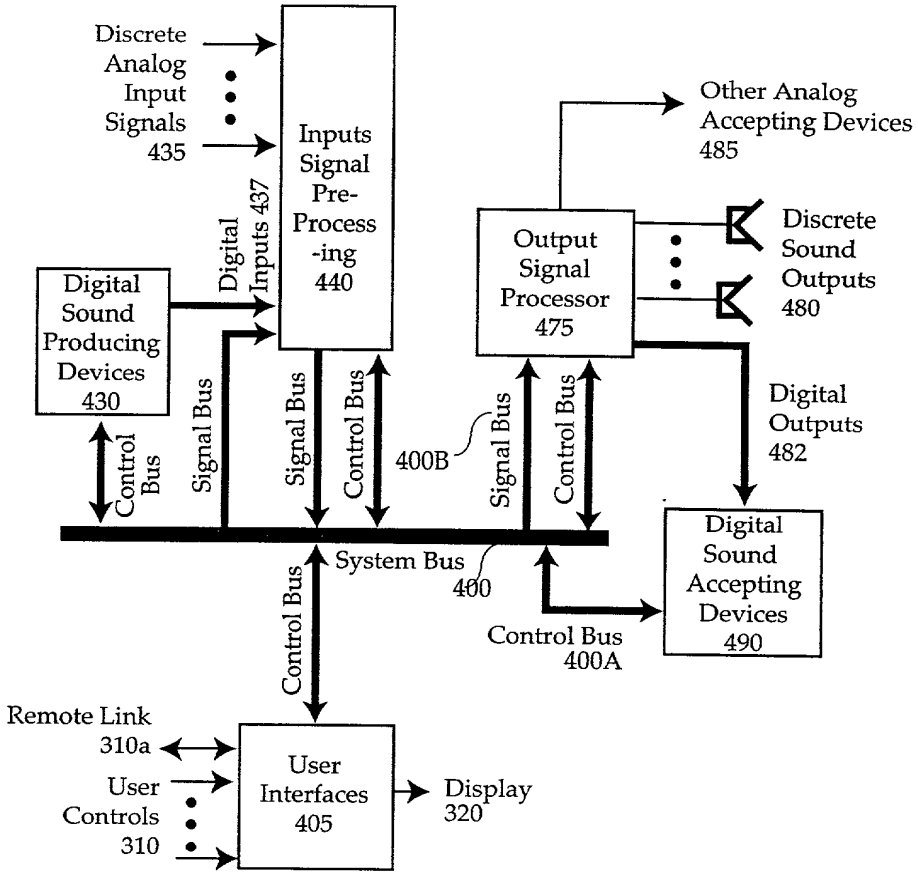

Discrete Analog Input Signals 435
Inputs Signal Pre-Process -ing 440
Digital Inputs 437
Other Analog Accepting Devices 485
Output Signal Processor 475
Discrete Sound Outputs 480
Digital Sound Producing Devices 430
Control Bus
Signal Bus
Signal Bus
Control Bus
400B
Signal Bus
Control Bus
Digital Outputs 482
System Bus 400
Control Bus 400A
Digital Sound Accepting Devices 490
Control Bus
Remote Link 310a
User Controls 310
User Interfaces 405
Display 320

FIG. 5E

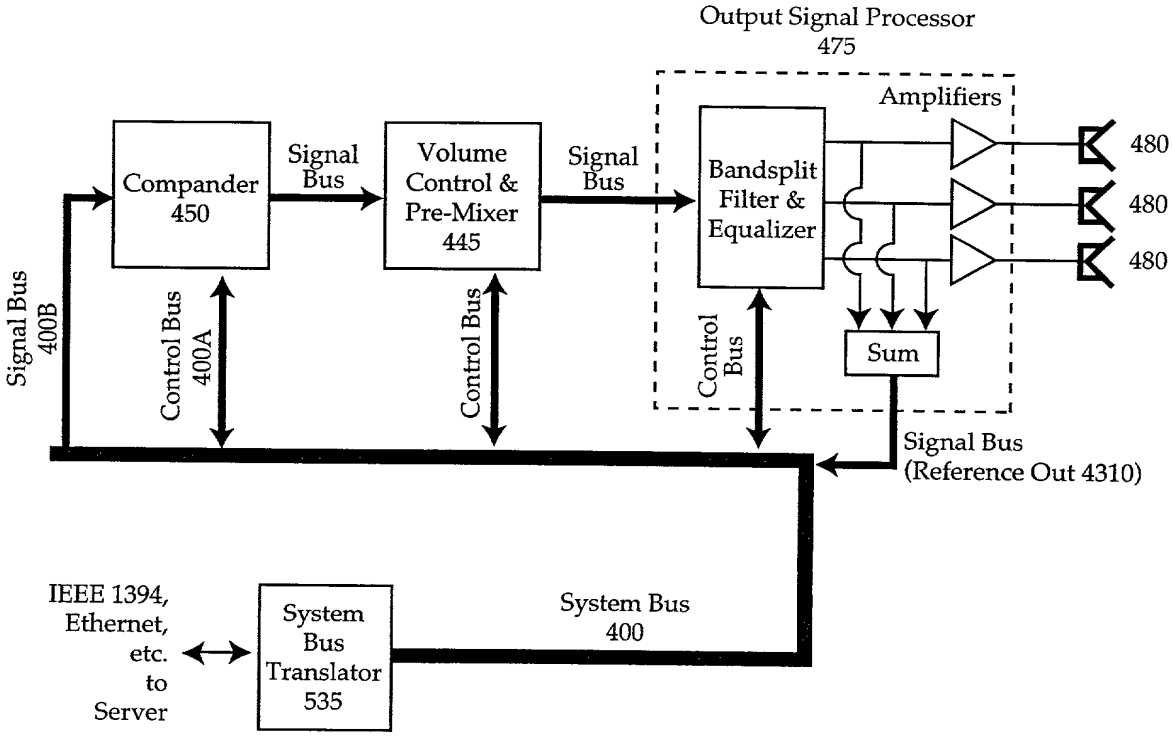

Output Signal Processor
475
Amplifiers
Compander
450
Signal
Bus
Volume
Control &
Pre-Mixer
445
Signal
Bus
Bandsplit
Filter &
Equalizer
480
480
480
Signal Bus
400B
Control Bus
400A
Control Bus
Control
Bus
Sum
Signal Bus
(Reference Out 4310)
IEEE 1394,
Ethernet,
etc.
to
Server
System
Bus
Translator
535
System Bus
400

FIG. 5F

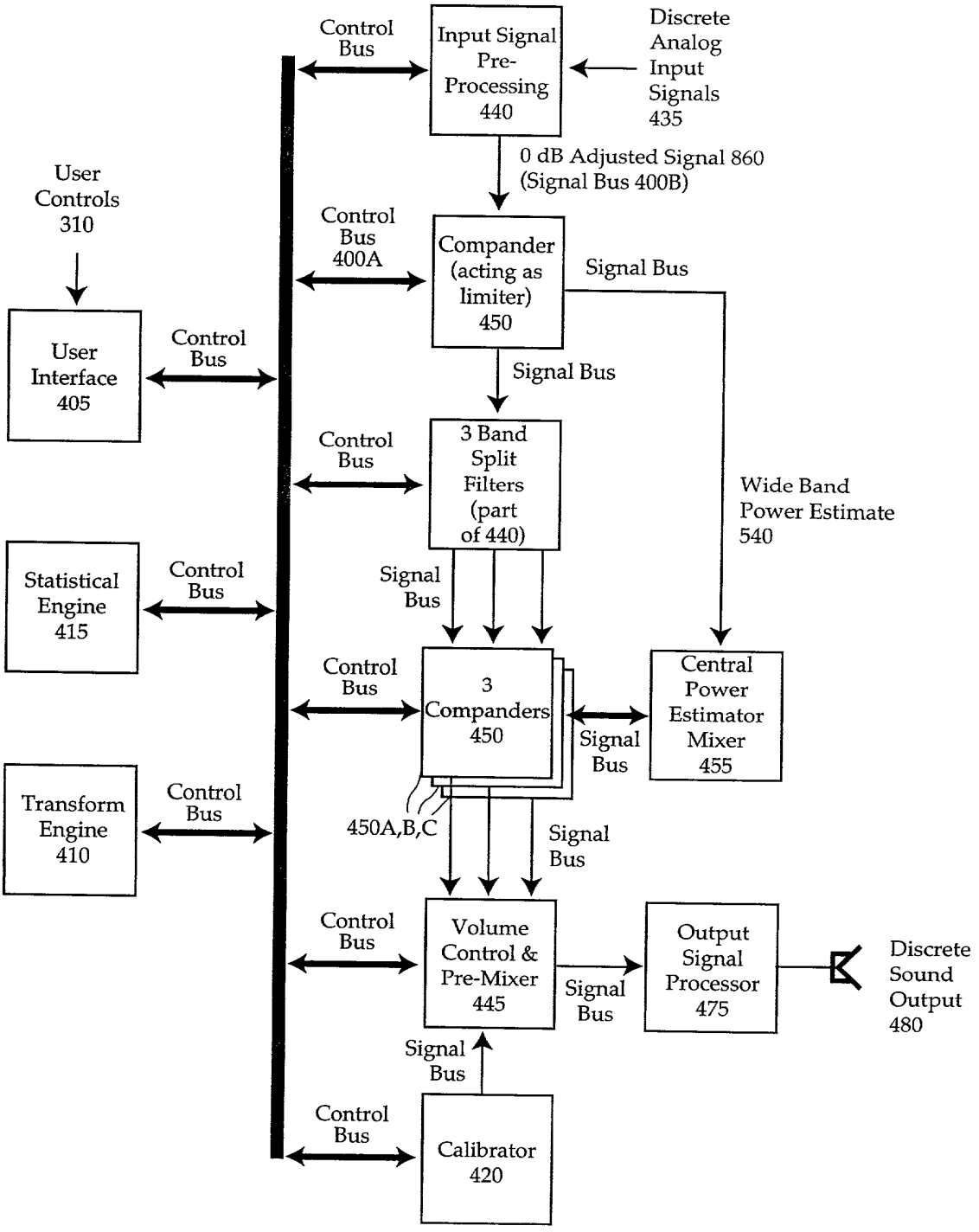

Control Bus
Input Signal Pre-Processing 440
Discrete Analog Input Signals 435
0 dB Adjusted Signal 860 (Signal Bus 400B)
User Controls 310
Control Bus 400A
Compander (acting as limiter) 450
Signal Bus
User Interface 405
Control Bus
Signal Bus
Control Bus
3 Band Split Filters (part of 440)
Wide Band Power Estimate 540
Statistical Engine 415
Control Bus
Signal Bus
Control Bus
3 Companders 450
Central Power Estimator Mixer 455
Signal Bus
Transform Engine 410
Control Bus
450A,B,C
Signal Bus
Control Bus
Volume Control & Pre-Mixer 445
Output Signal Processor 475
Signal Bus
Discrete Sound Output 480
Signal Bus
Control Bus
Calibrator 420

FIG. 5G

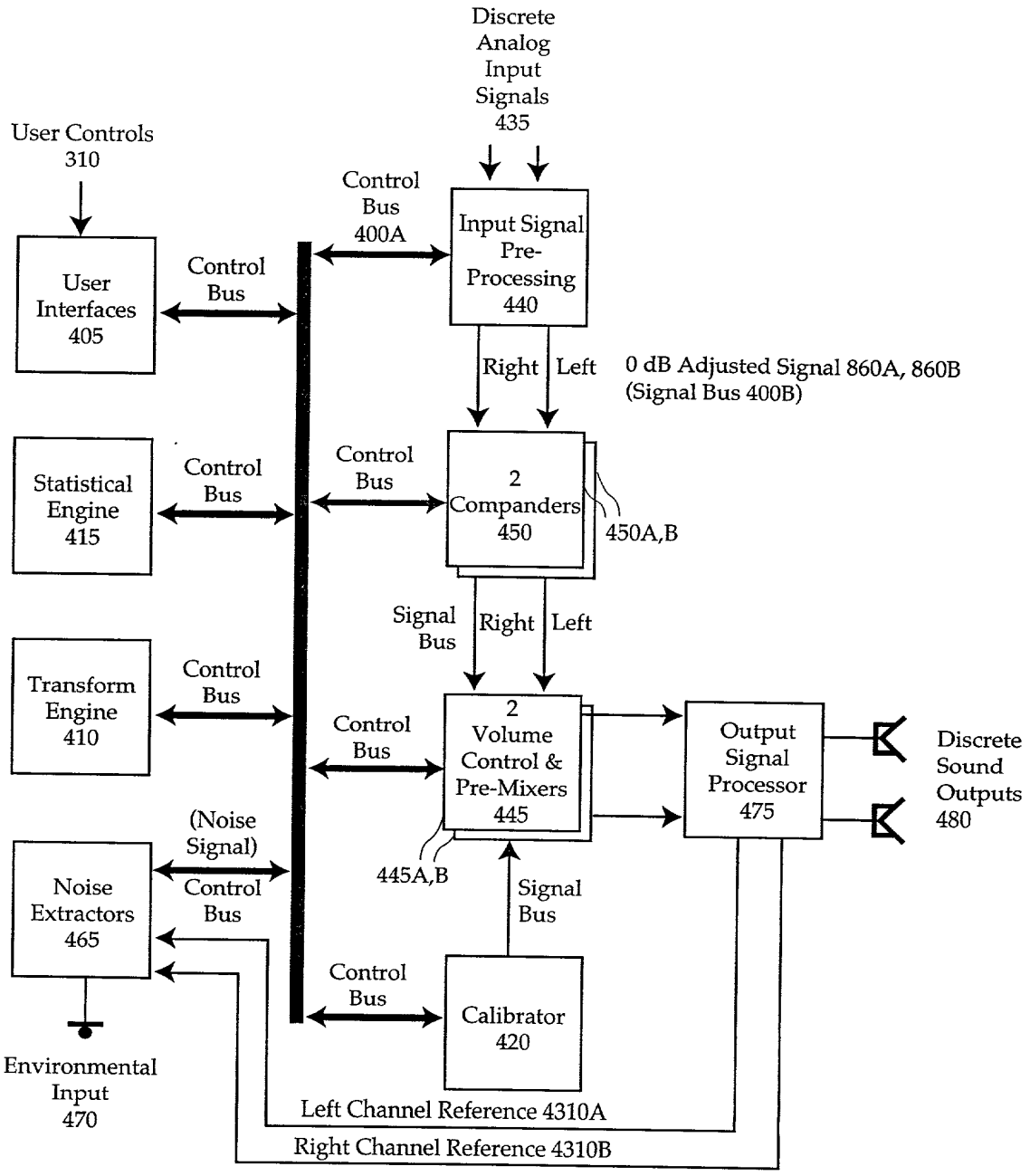

Discrete Analog Input Signals 435
User Controls 310
Control Bus 400A
Input Signal Pre-Processing 440
User Interfaces 405
Control Bus
Right
Left
0 dB Adjusted Signal 860A, 860B (Signal Bus 400B)
Statistical Engine 415
Control Bus
Control Bus
2 Companders 450
450A,B
Signal Bus
Right
Left
Transform Engine 410
Control Bus
Control Bus
2 Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
445A,B
(Noise Signal)
Noise Extractors 465
Control Bus
Signal Bus
Control Bus
Calibrator 420
Environmental Input 470
Left Channel Reference 4310A
Right Channel Reference 4310B

FIG. 5H

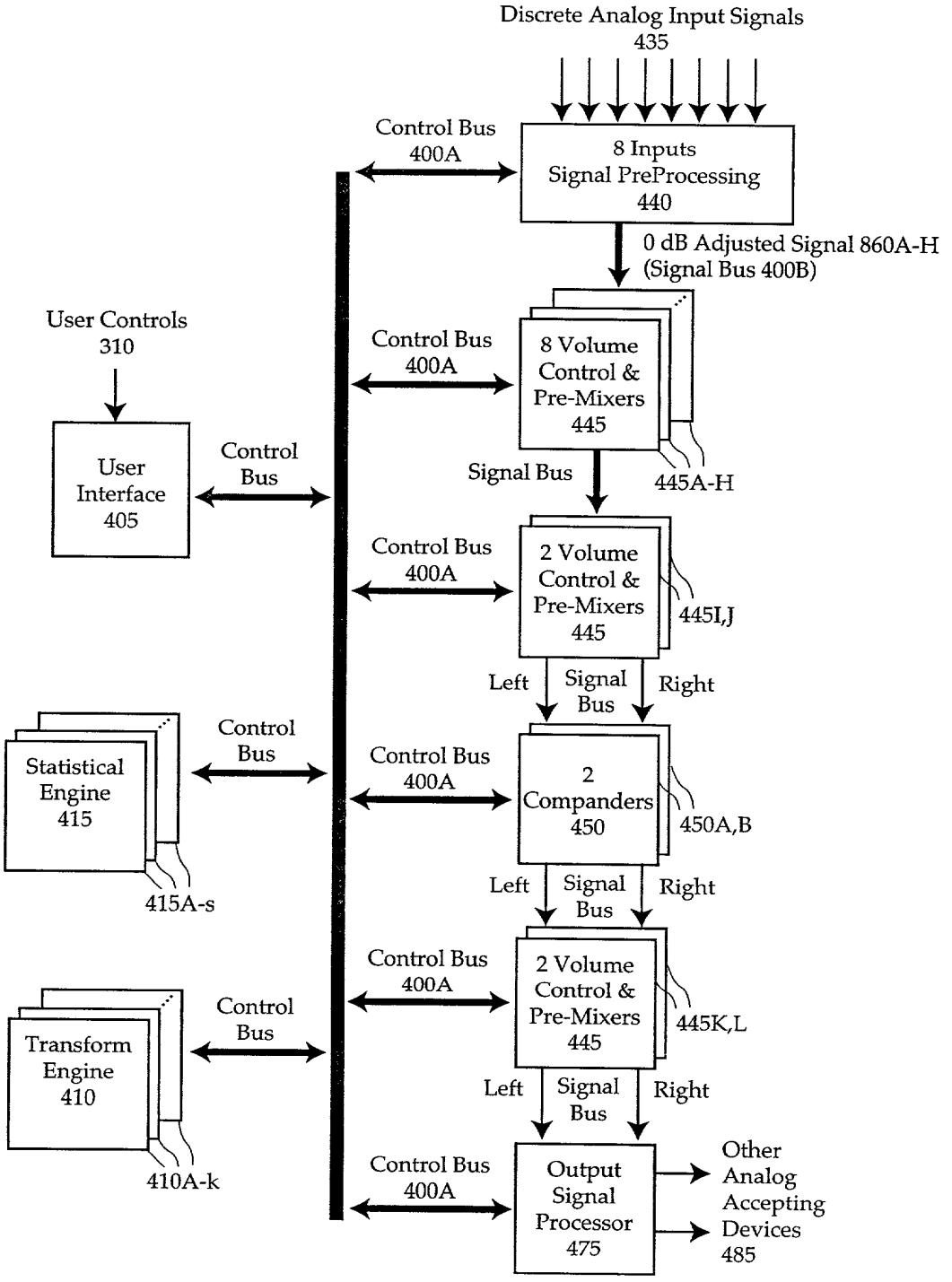

Discrete Analog Input Signals
435
Control Bus
400A
8 Inputs
Signal PreProcessing
440
0 dB Adjusted Signal 860A-H
(Signal Bus 400B)
User Controls
310
User
Interface
405
Control
Bus
Control Bus
400A
8 Volume
Control &
Pre-Mixers
445
445A-H
Signal Bus
Control Bus
400A
2 Volume
Control &
Pre-Mixers
445
445I,J
Left
Signal
Bus
Right
Statistical
Engine
415
415A-s
Control
Bus
Control Bus
400A
2
Companders
450
450A,B
Left
Signal
Bus
Right
Transform
Engine
410
410A-k
Control
Bus
Control Bus
400A
2 Volume
Control &
Pre-Mixers
445
445K,L
Left
Signal
Bus
Right
Control Bus
400A
Output
Signal
Processor
475
Other
Analog
Accepting
Devices
485

FIG. 5I

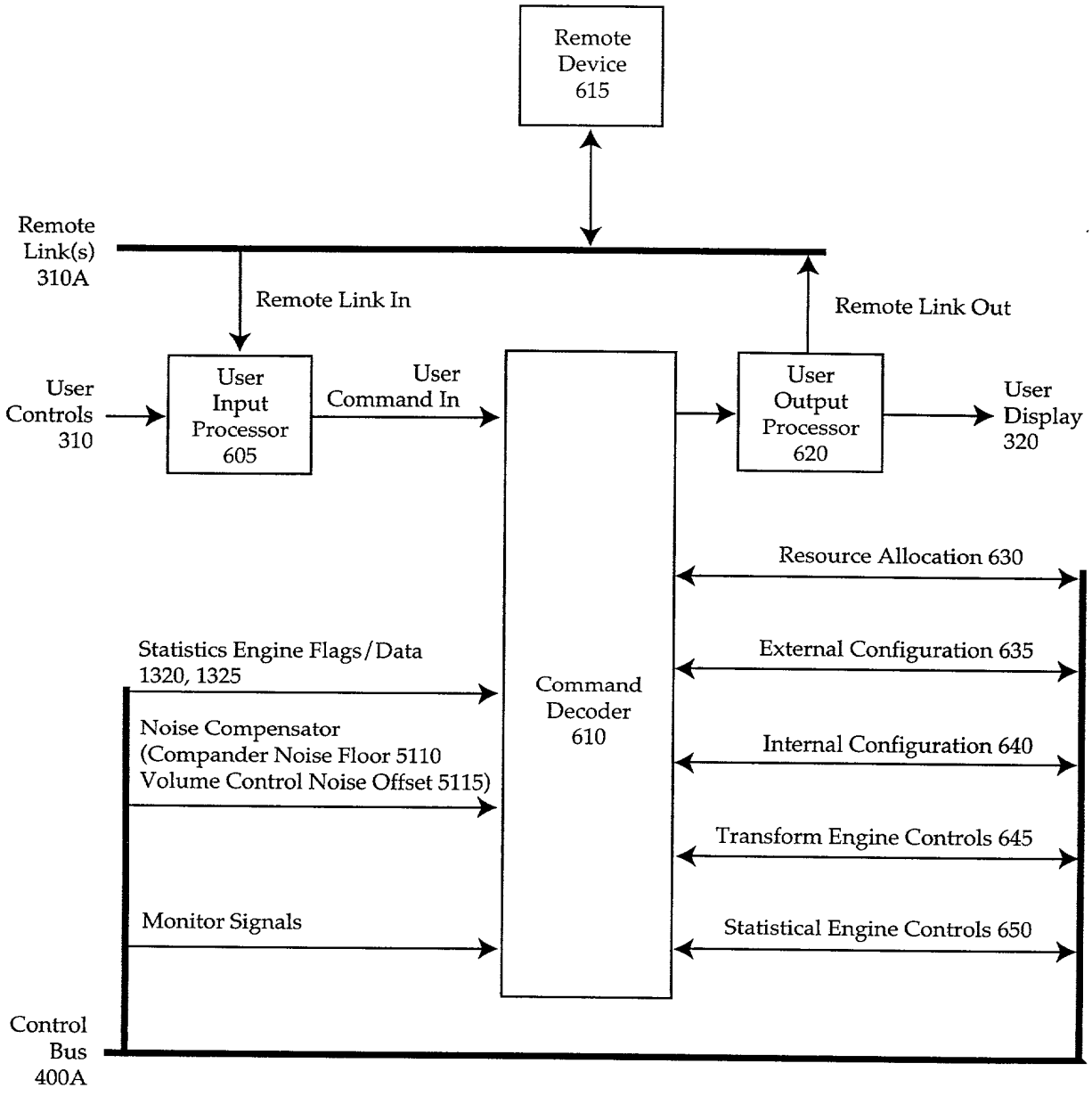

Remote Device 615
Remote Link(s) 310A
Remote Link In
Remote Link Out
User Controls 310
User Input Processor 605
User Command In
Command Decoder 610
User Output Processor 620
User Display 320
Resource Allocation 630
Statistics Engine Flags/Data 1320, 1325
External Configuration 635
Noise Compensator (Compander Noise Floor 5110 Volume Control Noise Offset 5115)
Internal Configuration 640
Transform Engine Controls 645
Monitor Signals
Statistical Engine Controls 650
Control Bus 400A

FIG. 6A

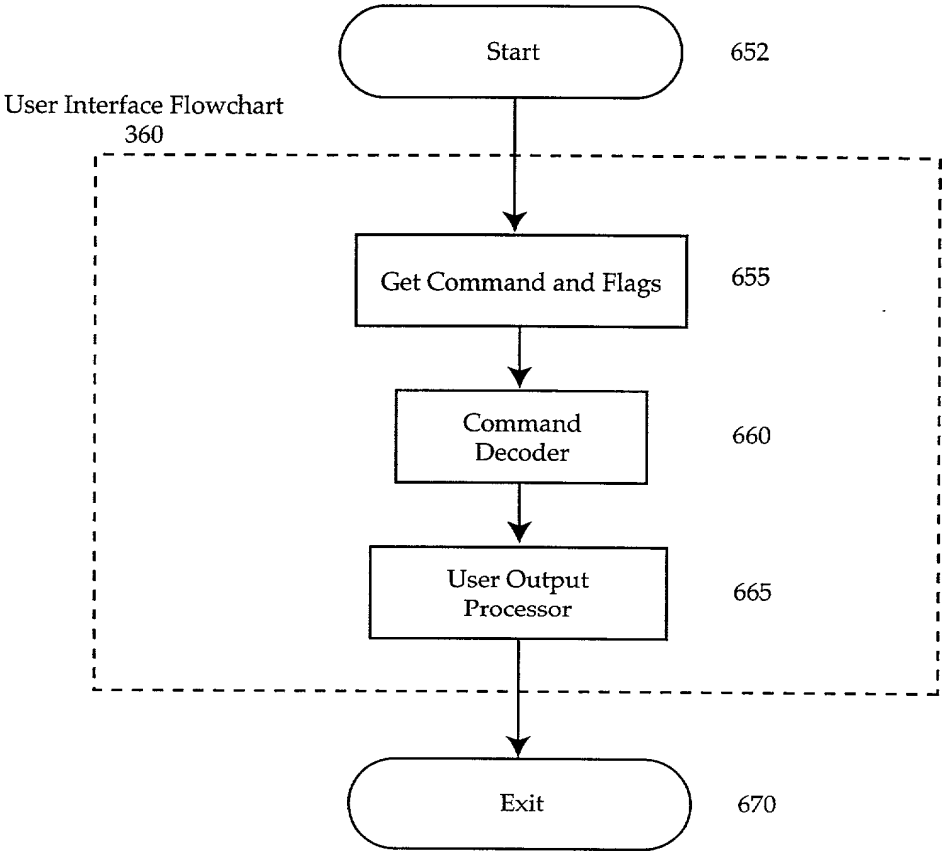

Start
652
User Interface Flowchart
360
Get Command and Flags
655
Command
Decoder
660
User Output
Processor
665
Exit
670

FIG. 6B

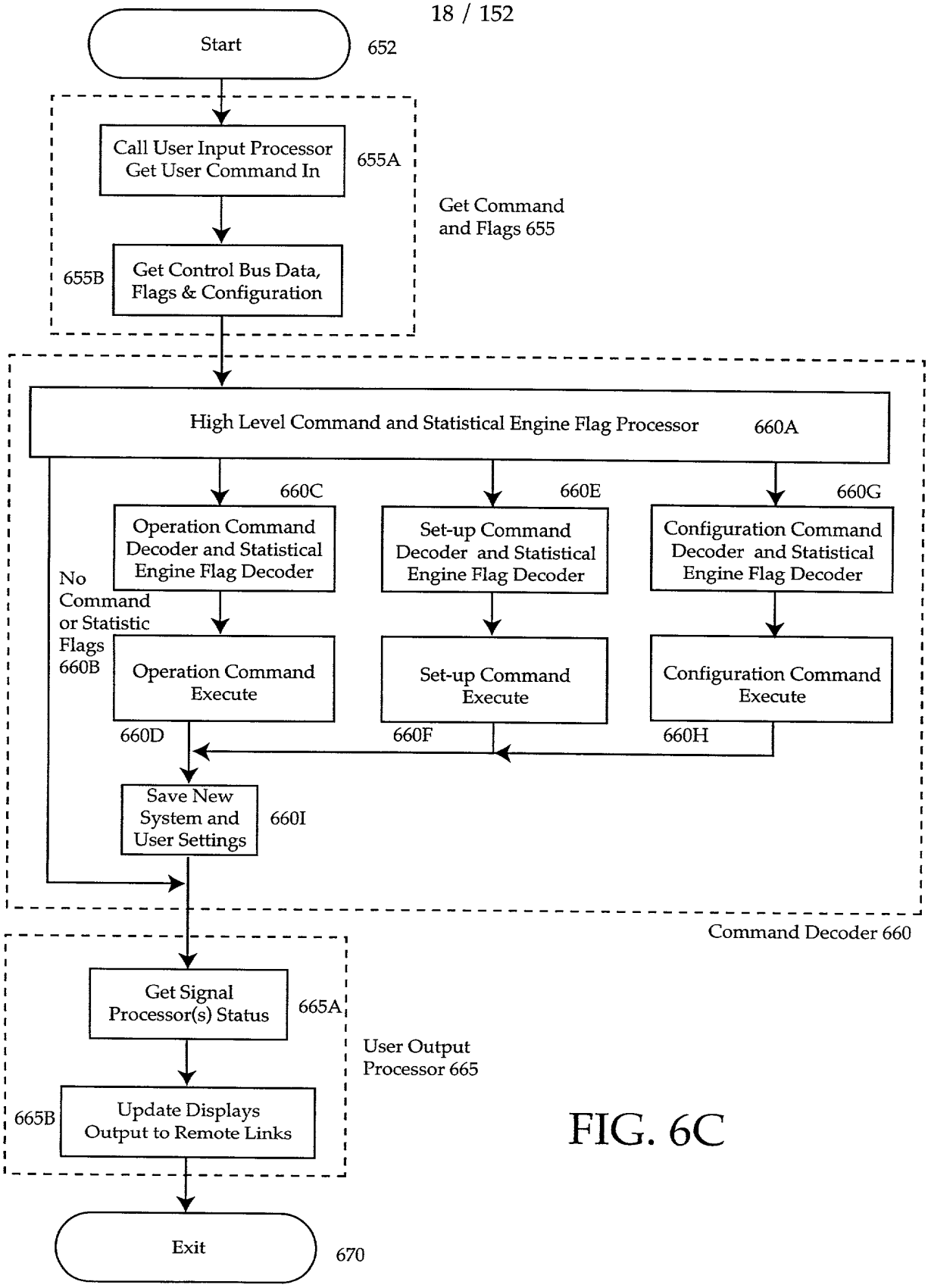

Start
652
Call User Input Processor Get User Command In
655A
Get Command and Flags 655
655B
Get Control Bus Data, Flags & Configuration
High Level Command and Statistical Engine Flag Processor
660A
660C
660E
660G
Operation Command Decoder and Statistical Engine Flag Decoder
Set-up Command Decoder and Statistical Engine Flag Decoder
Configuration Command Decoder and Statistical Engine Flag Decoder
No Command or Statistic Flags 660B
Operation Command Execute
Set-up Command Execute
Configuration Command Execute
660D
660F
660H
Save New System and User Settings
660I
Command Decoder 660
Get Signal Processor(s) Status
665A
User Output Processor 665
665B
Update Displays Output to Remote Links
Exit
670

FIG. 6C

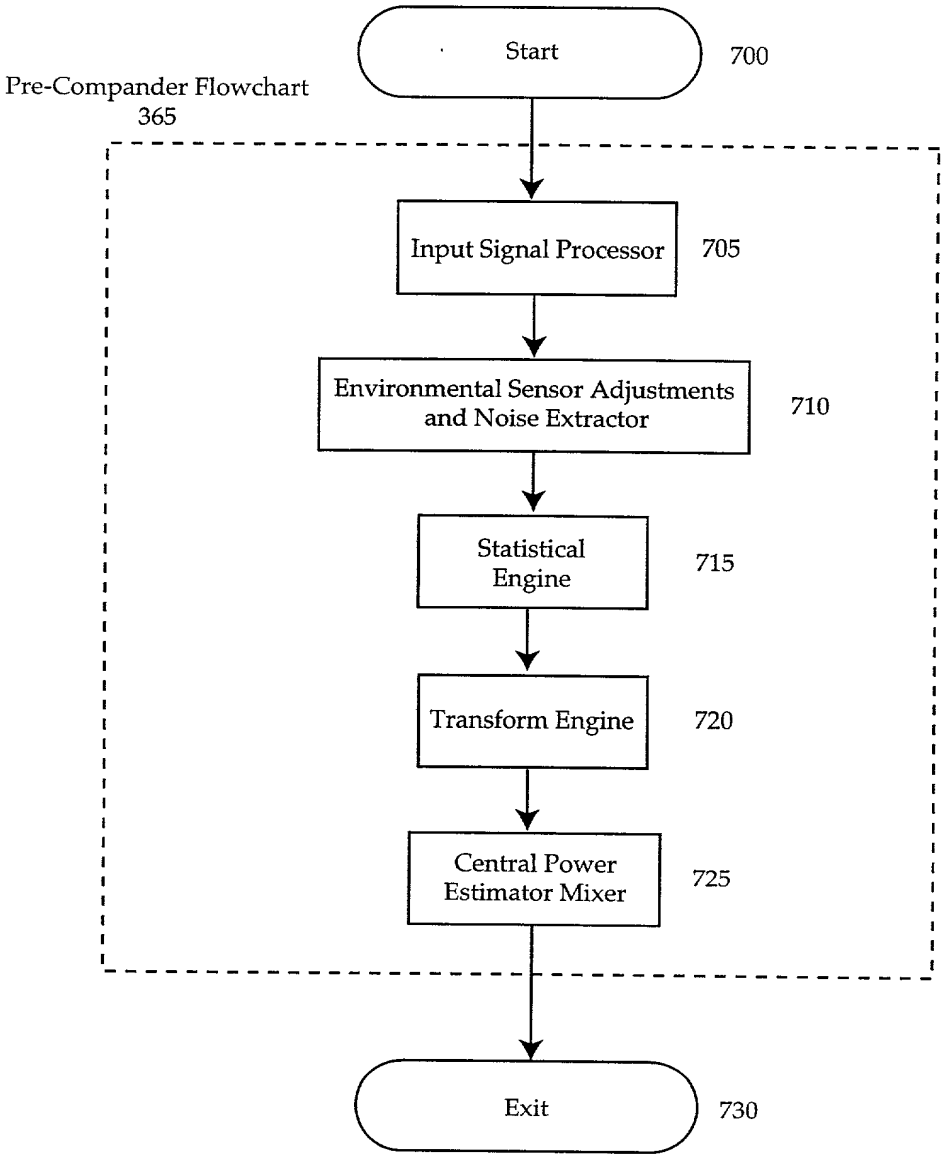

Pre-Compander Flowchart
365
Start
700
Input Signal Processor
705
Environmental Sensor Adjustments and Noise Extractor
710
Statistical Engine
715
Transform Engine
720
Central Power Estimator Mixer
725
Exit
730

FIG. 7

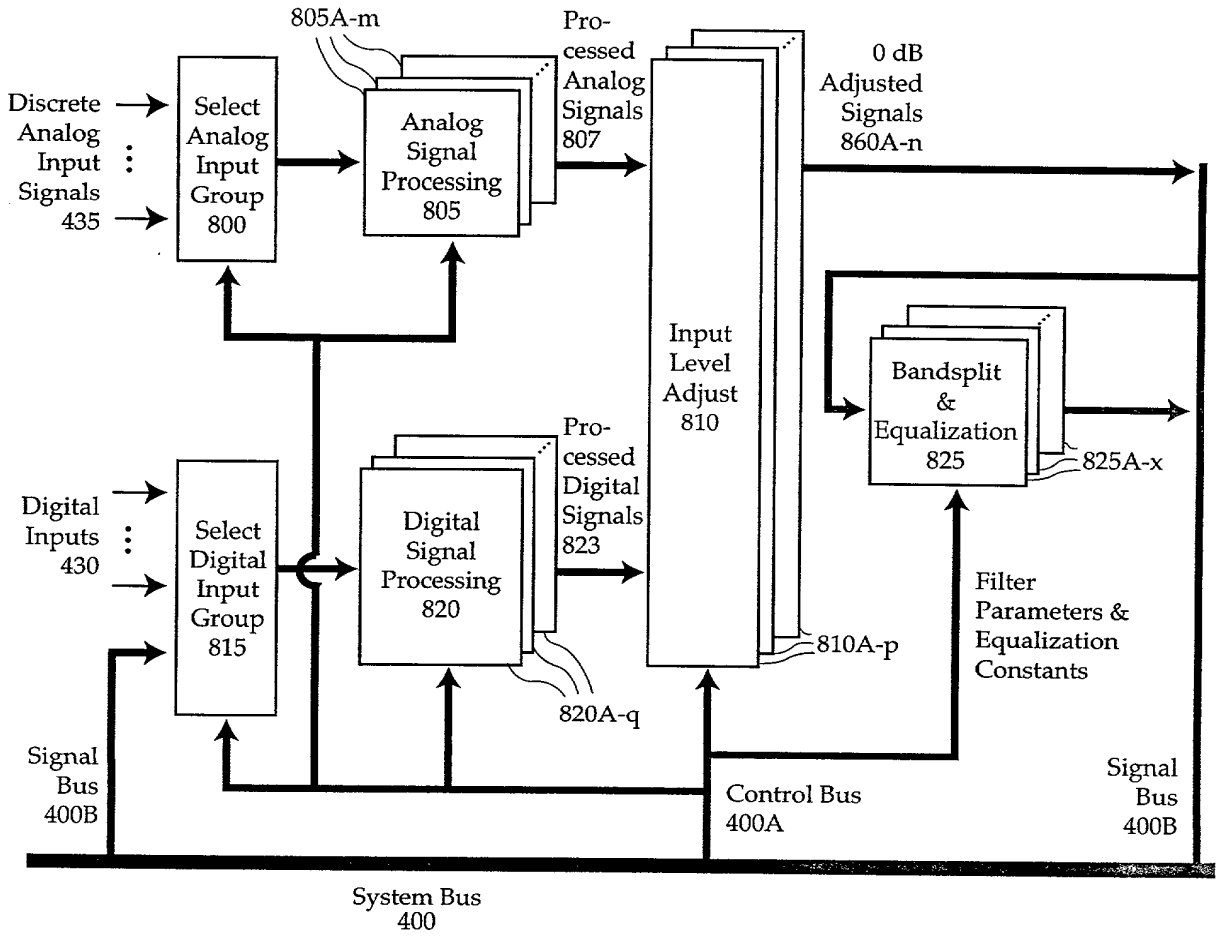

805A-m
Pro-
cessed
Analog
Signals
807
0 dB
Adjusted
Signals
860A-n
Discrete
Analog
Input
Signals
435
Select
Analog
Input
Group
800
Analog
Signal
Processing
805
Input
Level
Adjust
810
Bandsplit
&
Equalization
825
825A-x
Pro-
cessed
Digital
Signals
823
Digital
Inputs
430
Select
Digital
Input
Group
815
Digital
Signal
Processing
820
820A-q
810A-p
Filter
Parameters &
Equalization
Constants
Signal
Bus
400B
Control Bus
400A
Signal
Bus
400B
System Bus
400

FIG. 8A

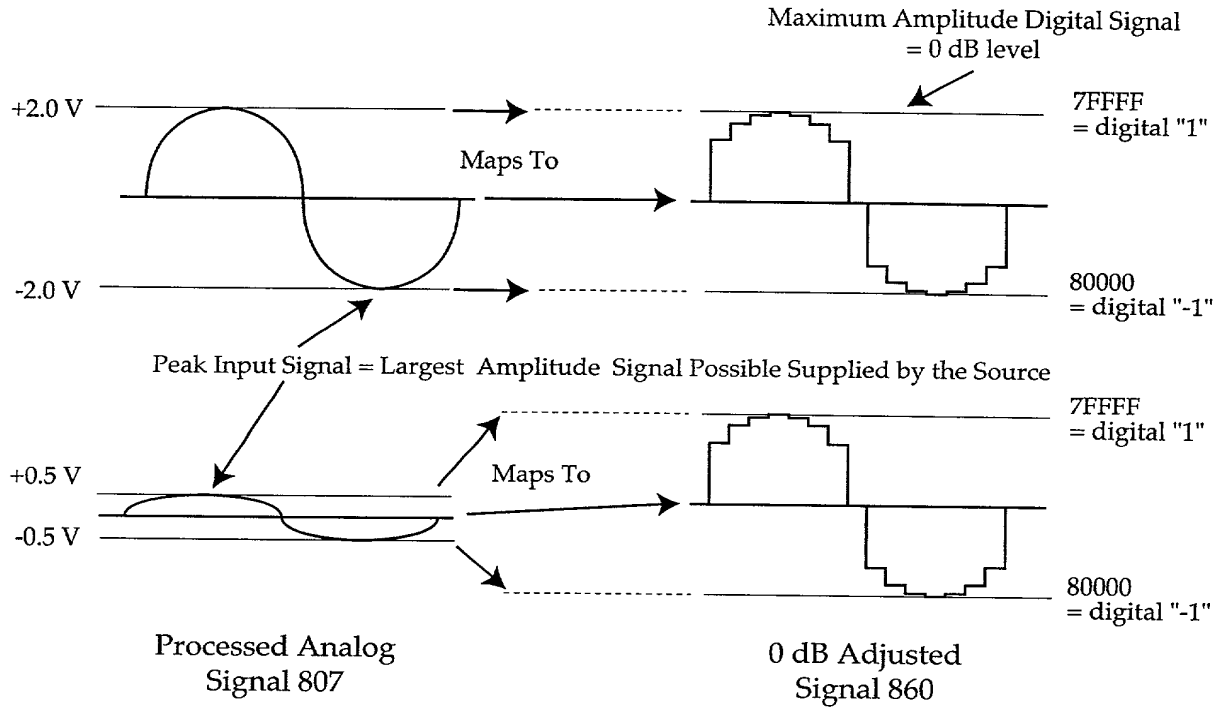

Maximum Amplitude Digital Signal
= 0 dB level
+2.0 V
-2.0 V
Maps To
7FFFF
= digital "1"
80000
= digital "-1"
Peak Input Signal = Largest Amplitude Signal Possible Supplied by the Source
+0.5 V
-0.5 V
Maps To
7FFFF
= digital "1"
80000
= digital "-1"
Processed Analog
Signal 807
0 dB Adjusted
Signal 860

FIG. 8B

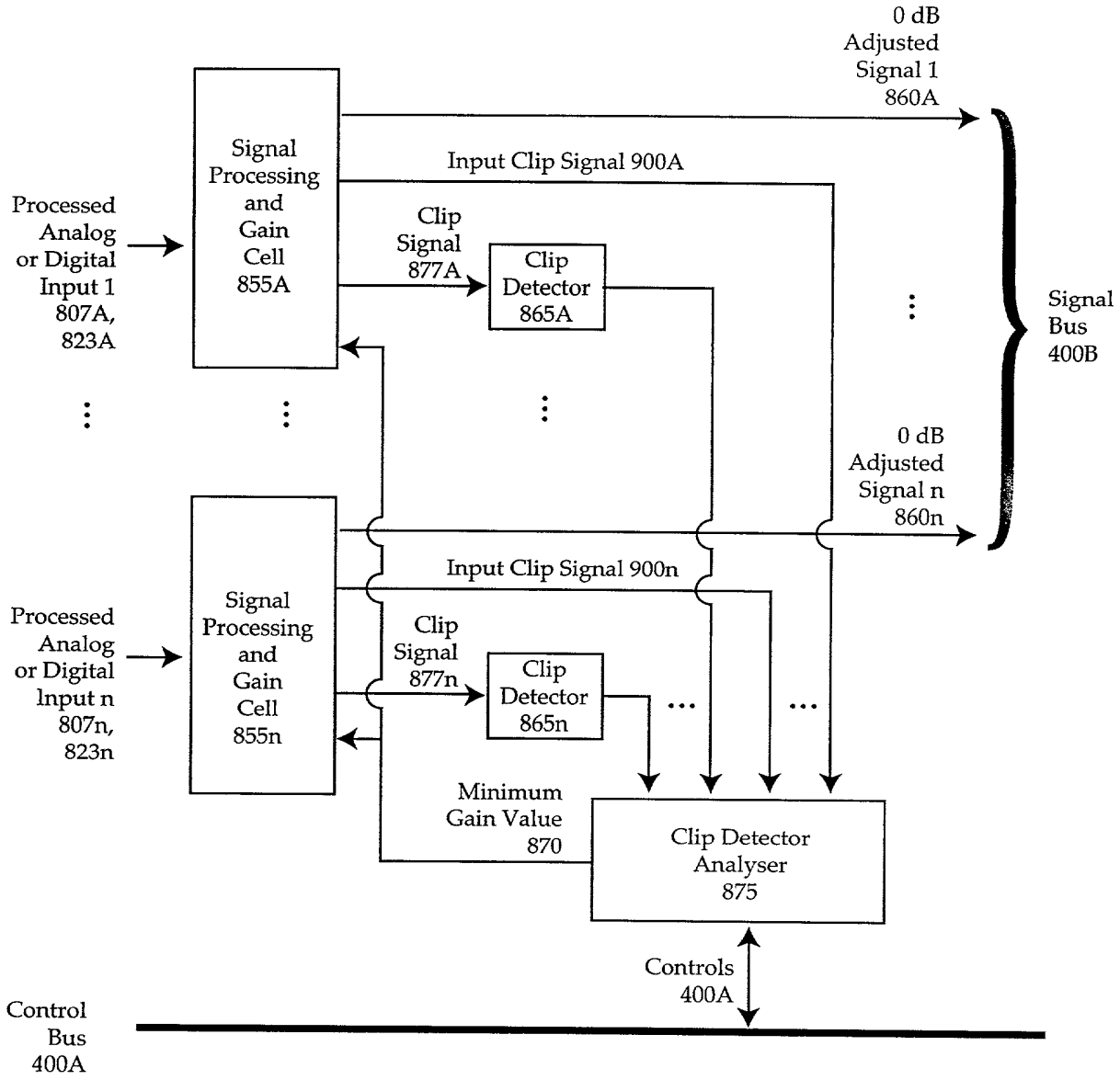

0 dB
Adjusted
Signal 1
860A
Signal
Processing
and
Gain
Cell
855A
Input Clip Signal 900A
Processed
Analog
or Digital
Input 1
807A,
823A
Clip
Signal
877A
Clip
Detector
865A
Signal
Bus
400B
0 dB
Adjusted
Signal n
860n
Input Clip Signal 900n
Signal
Processing
and
Gain
Cell
855n
Processed
Analog
or Digital
Input n
807n,
823n
Clip
Signal
877n
Clip
Detector
865n
Minimum
Gain Value
870
Clip Detector
Analyser
875
Controls
400A
Control
Bus
400A

FIG. 8C

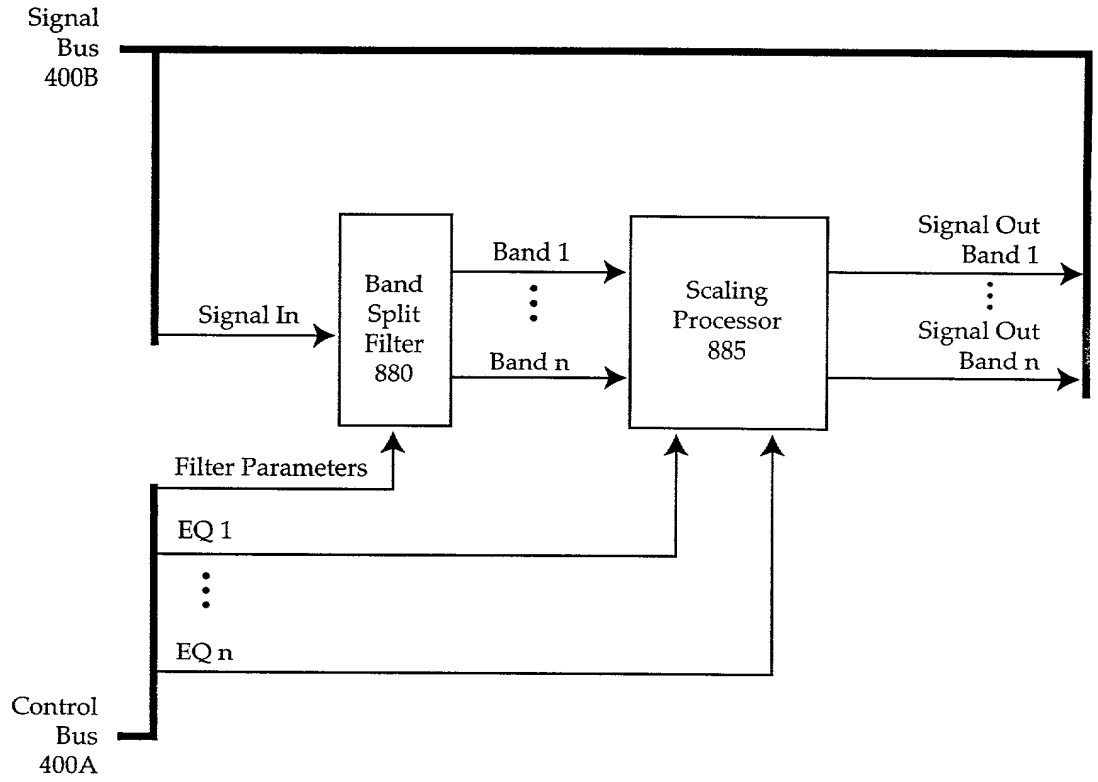

Signal
Bus
400B
Signal In
Band
Split
Filter
880
Band 1
Band n
Scaling
Processor
885
Signal Out
Band 1
Signal Out
Band n
Filter Parameters
EQ 1
EQ n
Control
Bus
400A

FIG. 8D

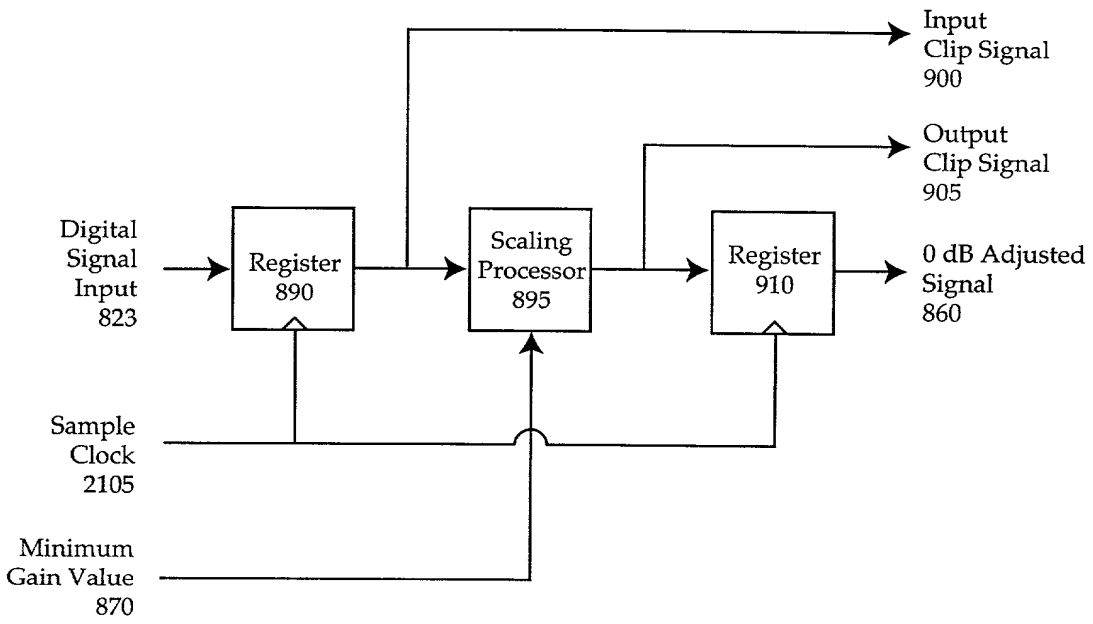

Input
Clip Signal
900
Output
Clip Signal
905
Digital
Signal
Input
823
Register
890
Scaling
Processor
895
Register
910
0 dB Adjusted
Signal
860
Sample
Clock
2105
Minimum
Gain Value
870

FIG. 8E

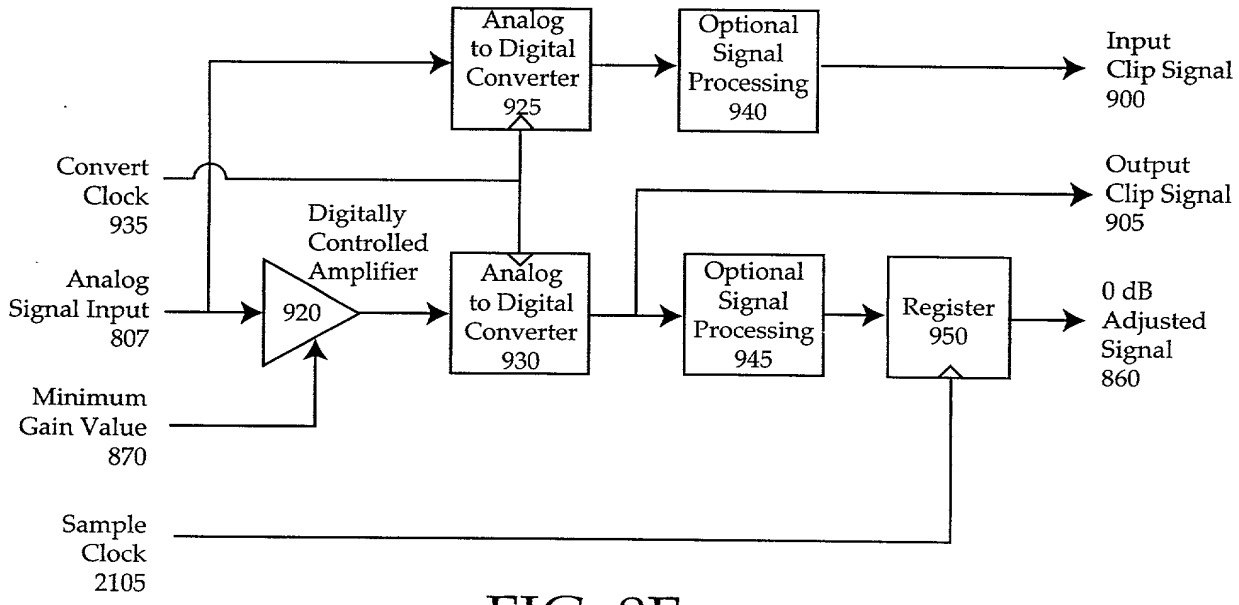

Analog
to Digital
Converter
925
Optional
Signal
Processing
940
Input
Clip Signal
900
Convert
Clock
935
Output
Clip Signal
905
Digitally
Controlled
Amplifier
Analog
Signal Input
807
920
Analog
to Digital
Converter
930
Optional
Signal
Processing
945
Register
950
0 dB
Adjusted
Signal
860
Minimum
Gain Value
870
Sample
Clock
2105

FIG. 8F

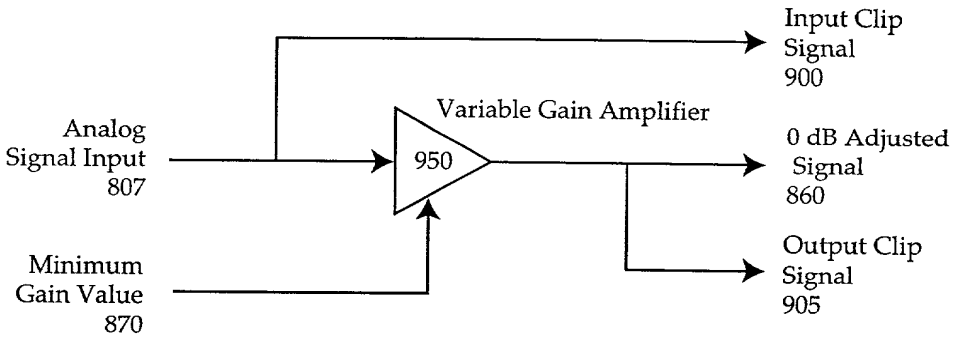


FIG. 8G

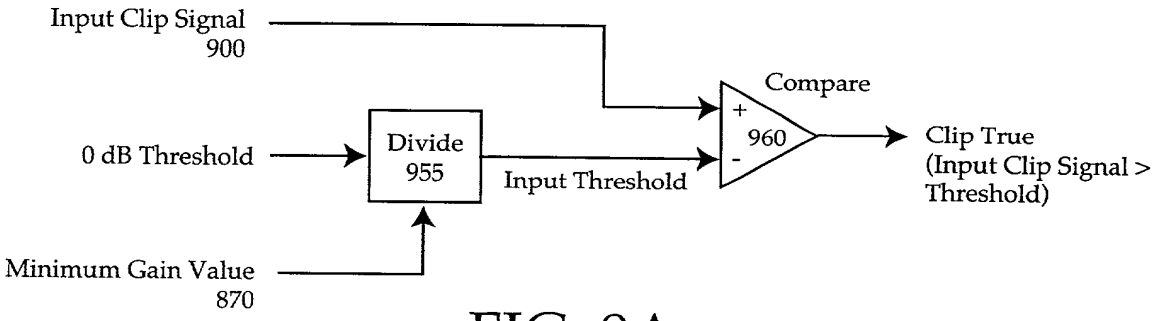


FIG. 9A

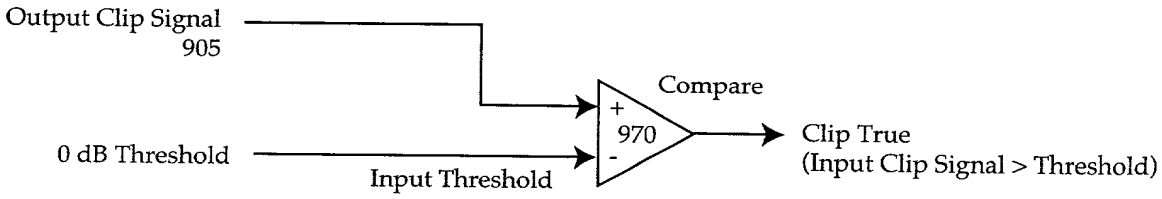


FIG. 9B

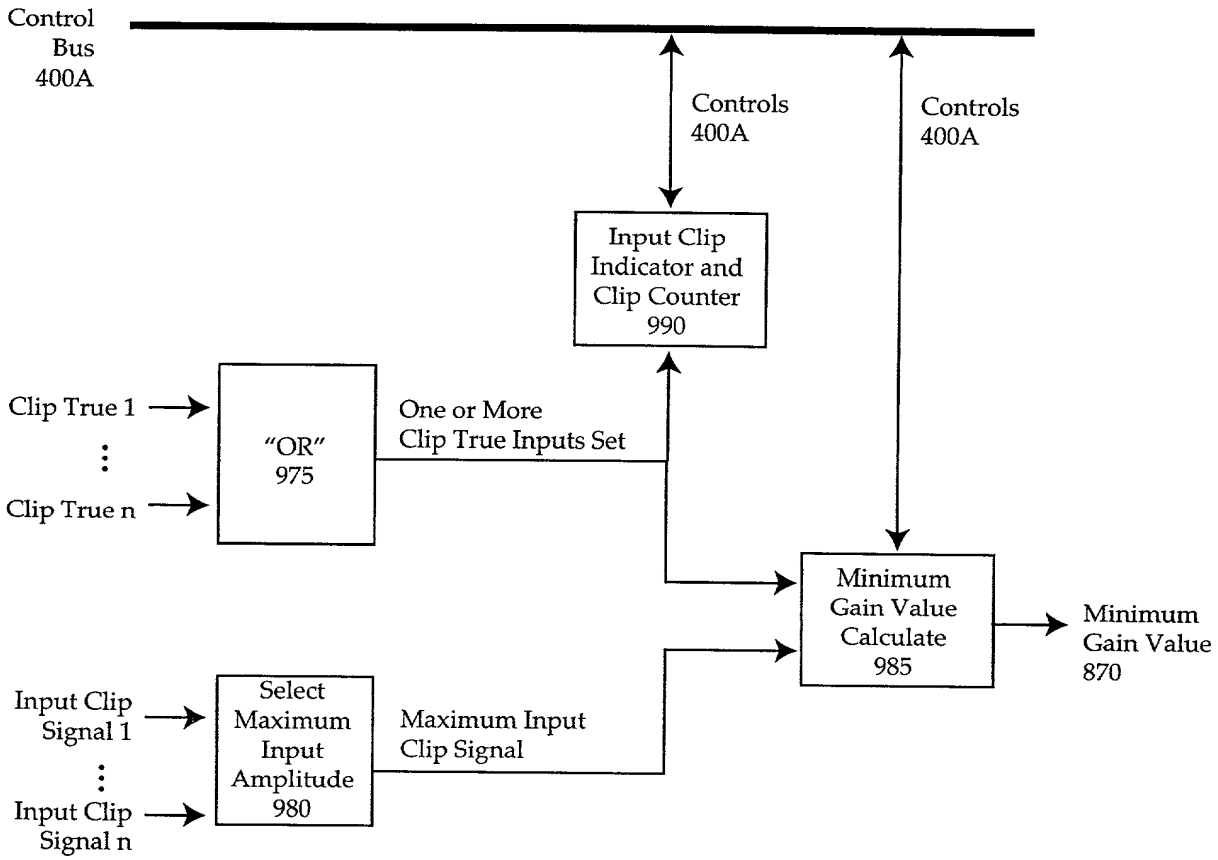

Control Bus 400A
Controls 400A
Controls 400A
Input Clip Indicator and Clip Counter 990
Clip True 1
Clip True n
"OR" 975
One or More Clip True Inputs Set
Minimum Gain Value Calculate 985
Minimum Gain Value 870
Input Clip Signal 1
Input Clip Signal n
Select Maximum Input Amplitude 980
Maximum Input Clip Signal

FIG. 9C

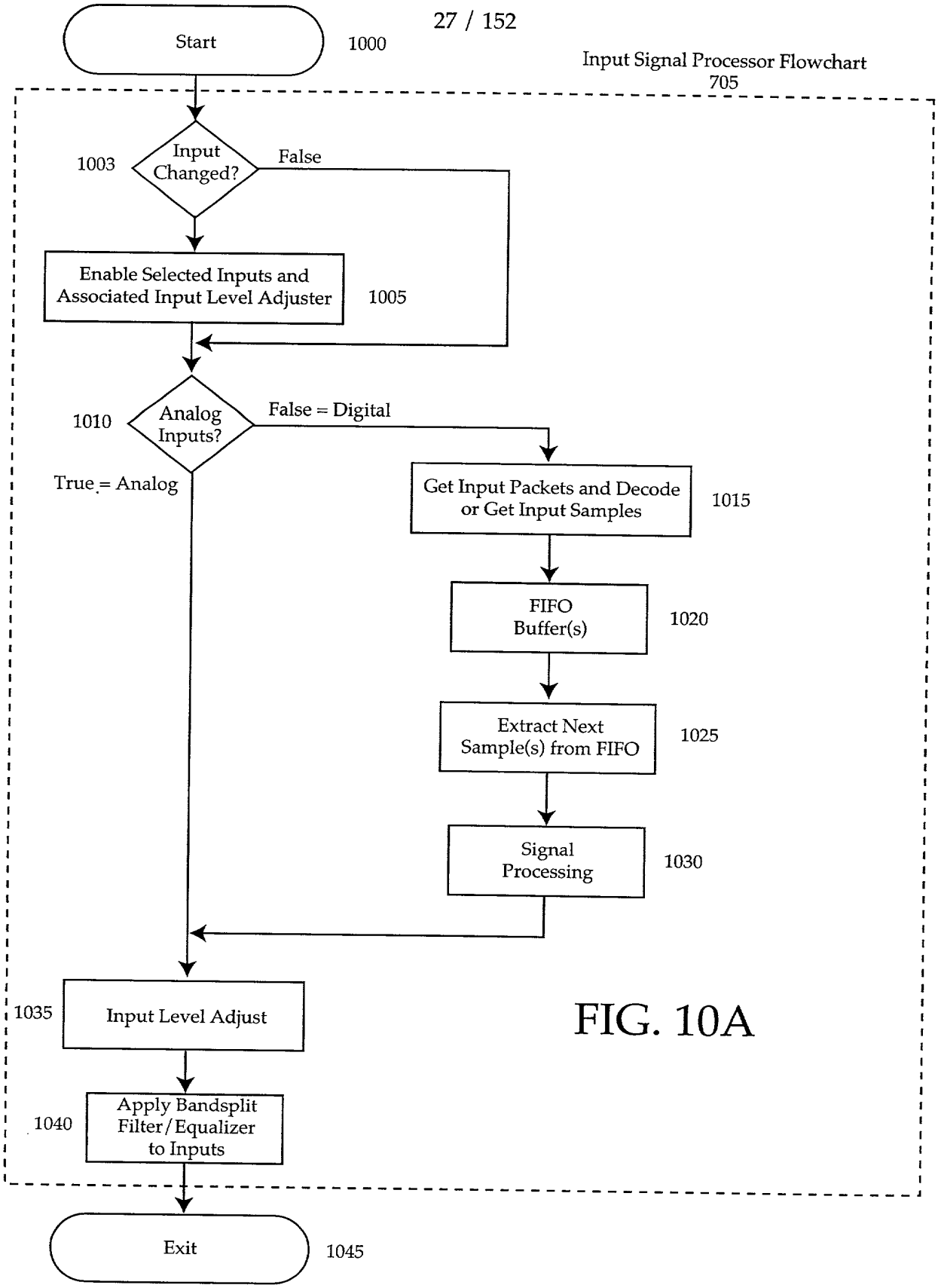

Start
1000
Input Signal Processor Flowchart
705
1003
Input Changed?
False
Enable Selected Inputs and Associated Input Level Adjuster
1005
1010
Analog Inputs?
False = Digital
True = Analog
Get Input Packets and Decode or Get Input Samples
1015
FIFO Buffer(s)
1020
Extract Next Sample(s) from FIFO
1025
Signal Processing
1030
1035
Input Level Adjust
1040
Apply Bandsplit Filter/Equalizer to Inputs
Exit
1045

FIG. 10A

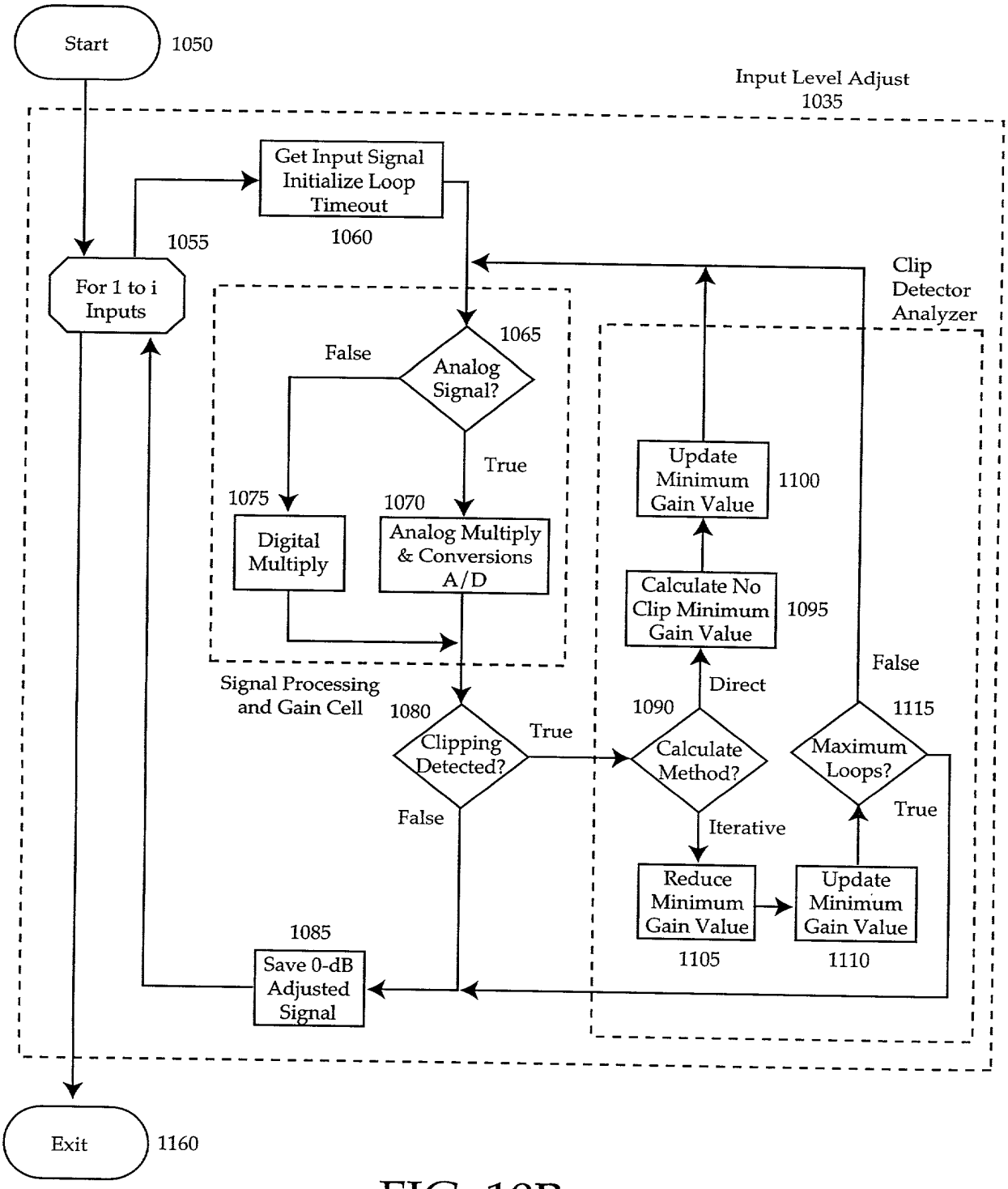

Start
1050
Input Level Adjust
1035
Get Input Signal
Initialize Loop
Timeout
1060
1055
For 1 to i
Inputs
Clip
Detector
Analyzer
1065
False
Analog
Signal?
True
1075
Digital
Multiply
1070
Analog Multiply
& Conversions
A/D
Signal Processing
and Gain Cell
1080
Clipping
Detected?
True
False
1090
Calculate
Method?
Direct
Iterative
Update
Minimum
Gain Value
1100
Calculate No
Clip Minimum
Gain Value
1095
Reduce
Minimum
Gain Value
1105
Update
Minimum
Gain Value
1110
1115
Maximum
Loops?
False
True
1085
Save 0-dB
Adjusted
Signal
Exit
1160

FIG. 10B

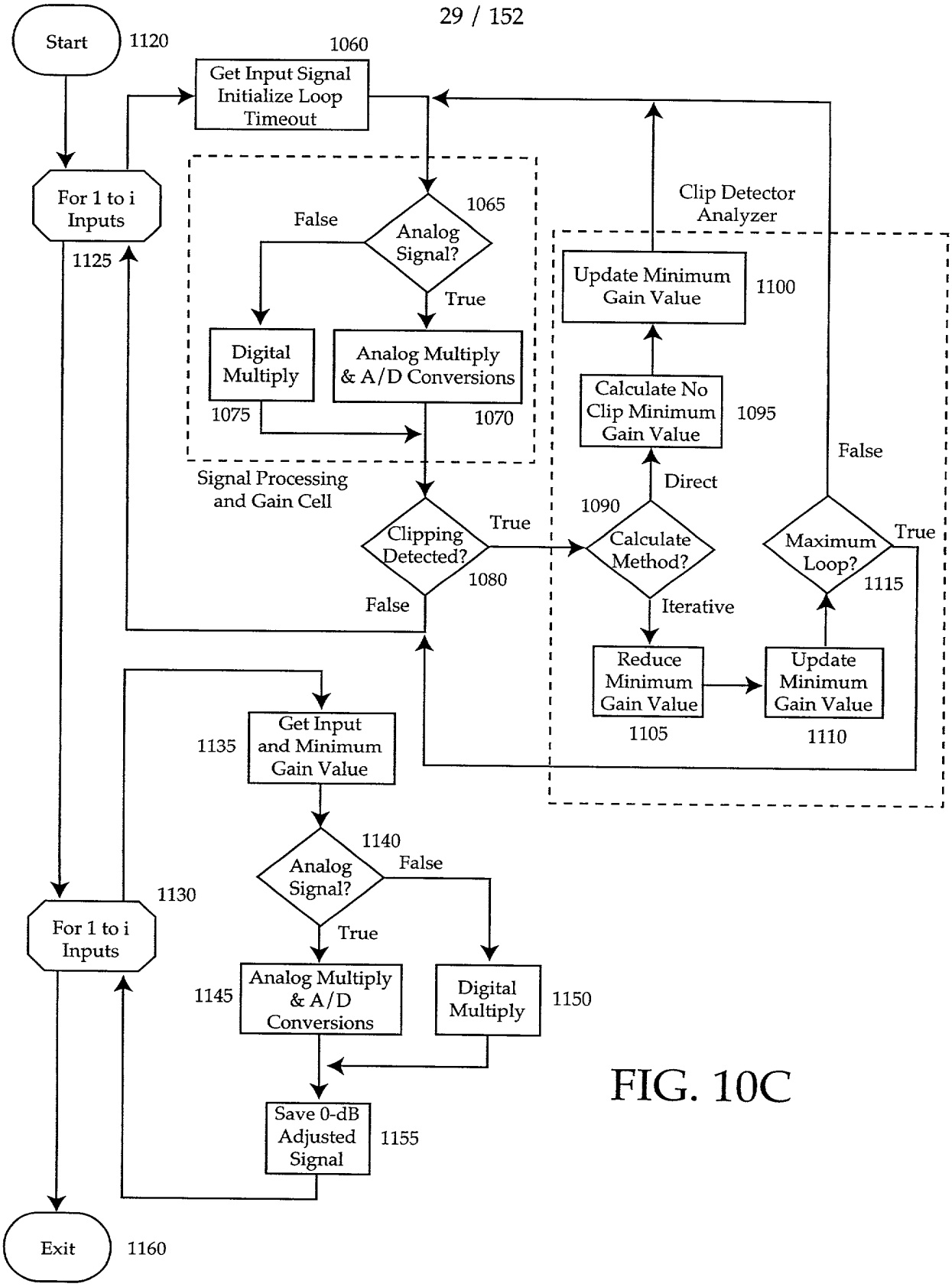

Start
1120
1060
Get Input Signal Initialize Loop Timeout
For 1 to i Inputs
1125
1065
Analog Signal?
False
True
Digital Multiply
Analog Multiply & A/D Conversions
1075
1070
Signal Processing and Gain Cell
Clip Detector Analyzer
Update Minimum Gain Value
1100
Calculate No Clip Minimum Gain Value
1095
Direct
1090
Calculate Method?
Clipping Detected?
True
1080
False
Iterative
Reduce Minimum Gain Value
1105
Update Minimum Gain Value
1110
Maximum Loop?
1115
True
False
1135
Get Input and Minimum Gain Value
1140
Analog Signal?
False
True
1130
For 1 to i Inputs
1145
Analog Multiply & A/D Conversions
Digital Multiply
1150
Save 0-dB Adjusted Signal
1155
Exit
1160

FIG. 10C

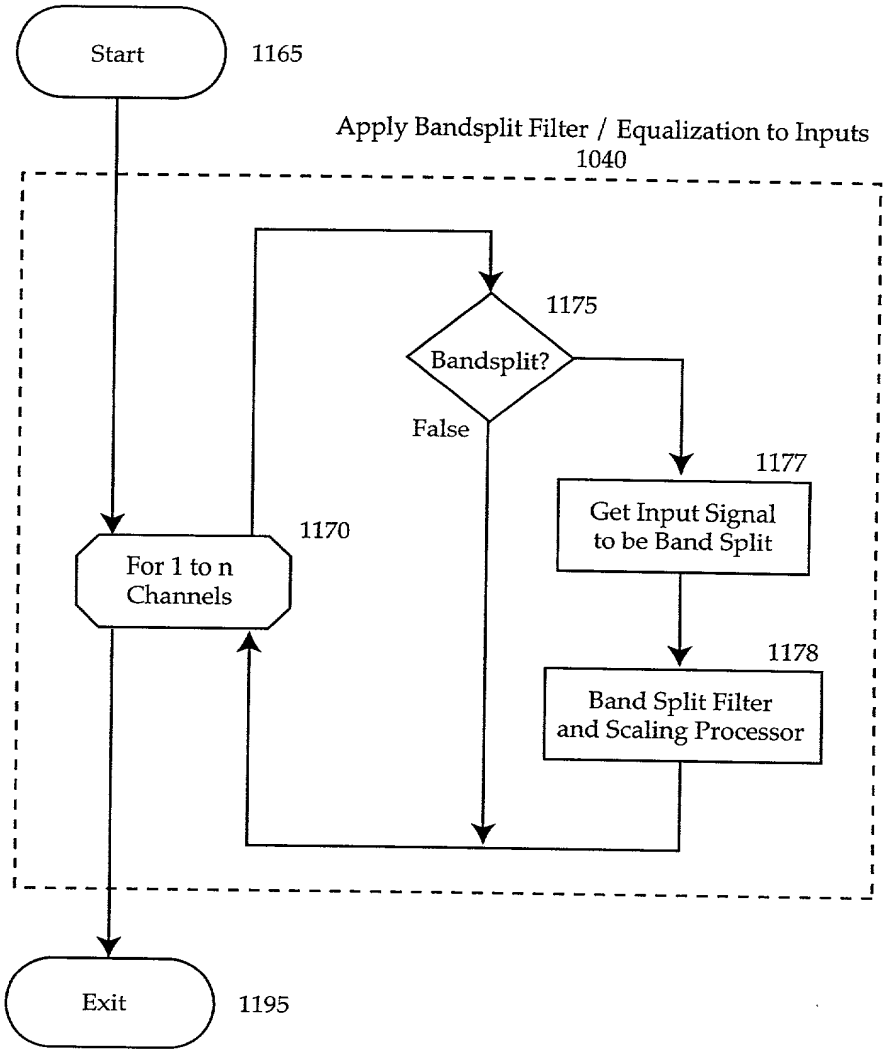

Start
1165
Apply Bandsplit Filter / Equalization to Inputs
1040
1175
Bandsplit?
False
1177
Get Input Signal
to be Band Split
1178
Band Split Filter
and Scaling Processor
1170
For 1 to n
Channels
Exit
1195

FIG. 10D

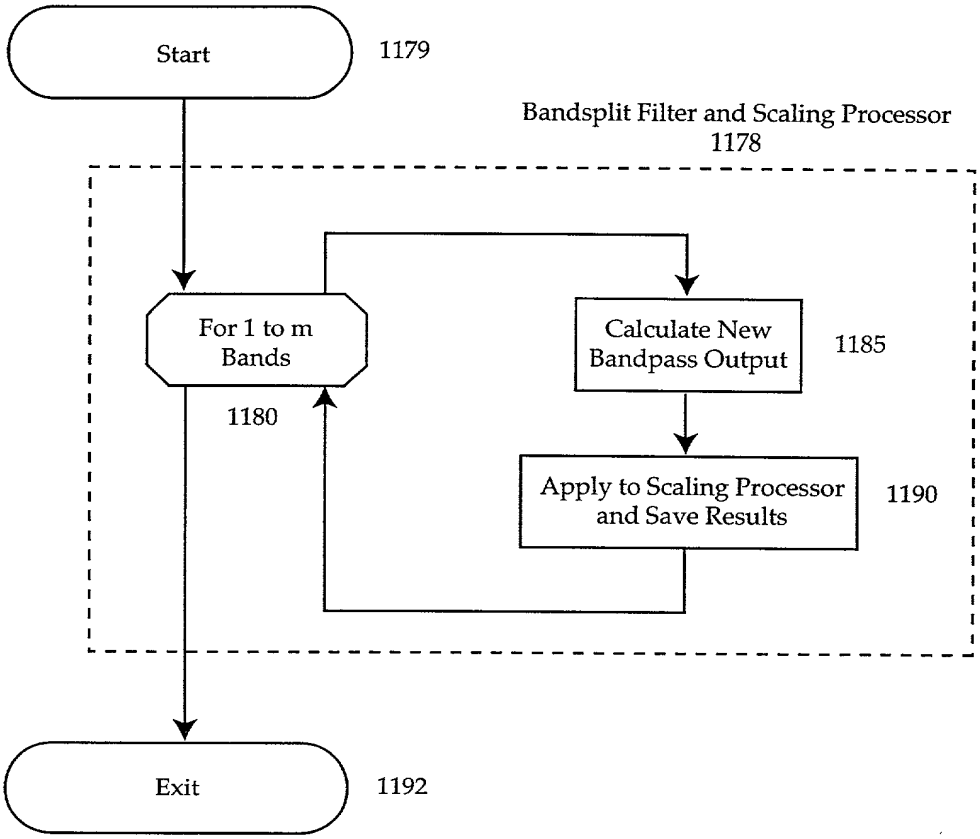

Start
1179
Bandsplit Filter and Scaling Processor
1178
For 1 to m
Bands
1180
Calculate New
Bandpass Output
1185
Apply to Scaling Processor
and Save Results
1190
Exit
1192

FIG. 10E

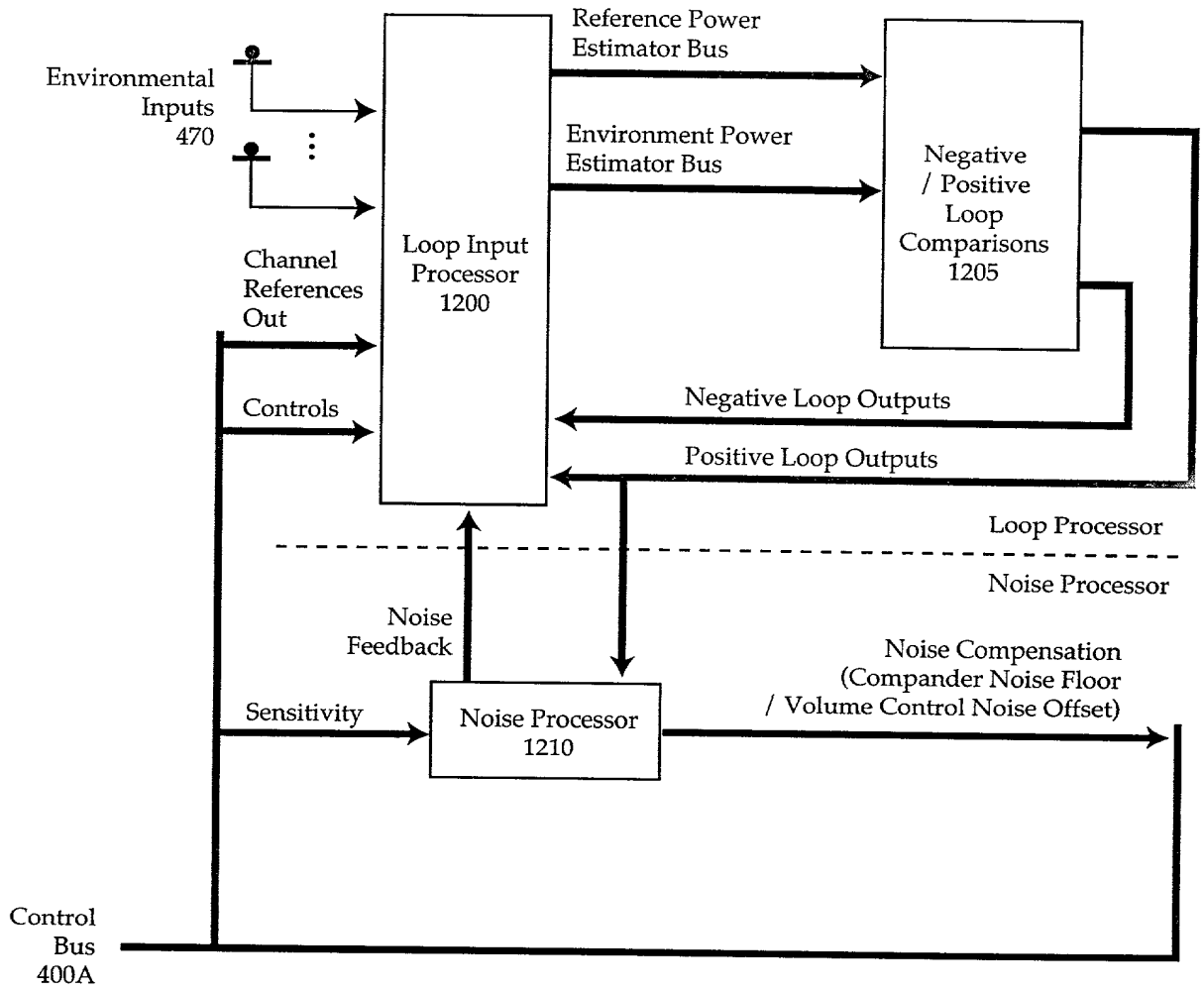

Environmental Inputs 470
Loop Input Processor 1200
Reference Power Estimator Bus
Environment Power Estimator Bus
Negative / Positive Loop Comparisons 1205
Channel References Out
Controls
Negative Loop Outputs
Positive Loop Outputs
Loop Processor
Noise Processor
Noise Feedback
Noise Compensation (Compander Noise Floor / Volume Control Noise Offset)
Sensitivity
Noise Processor 1210
Control Bus 400A

FIG. 11

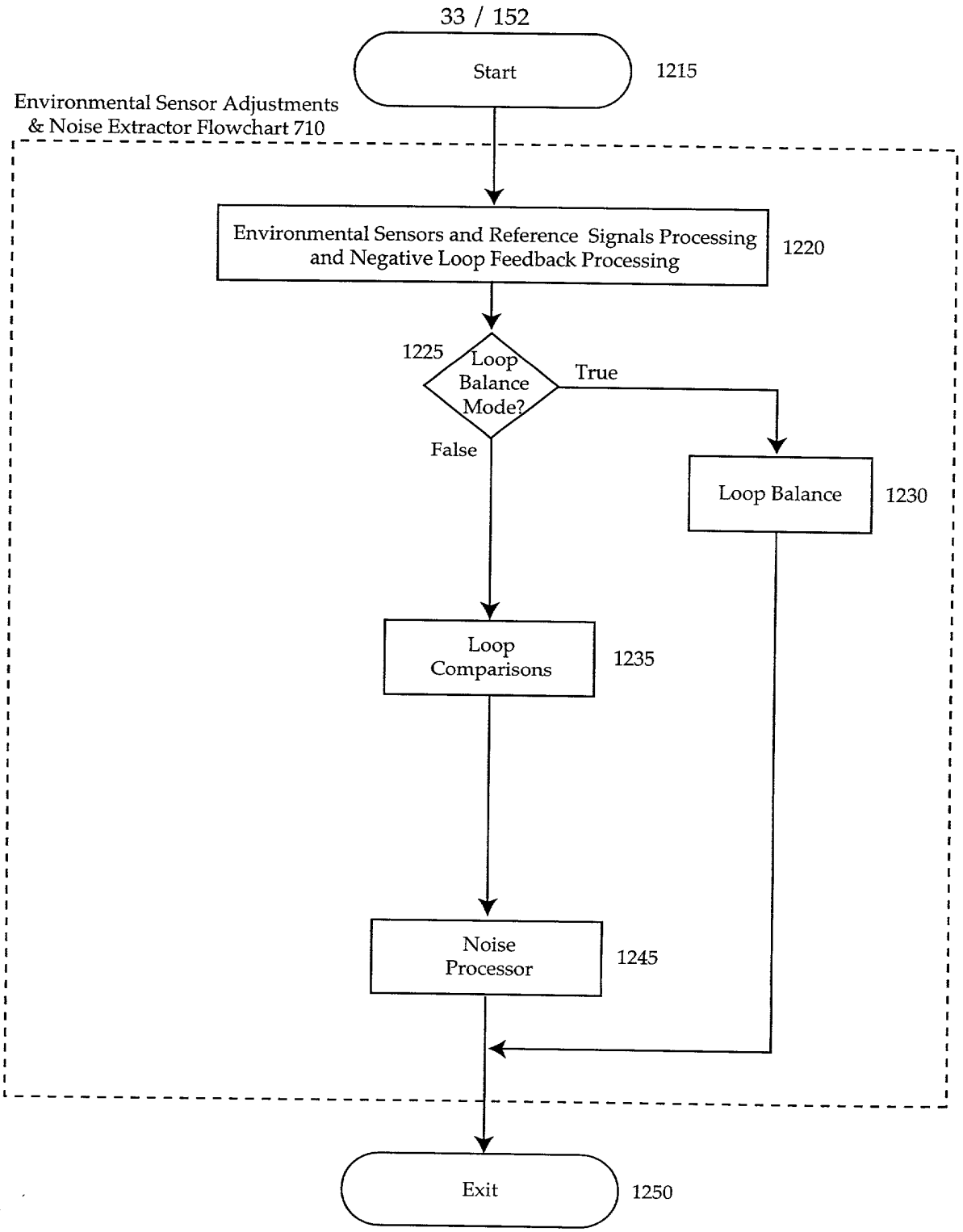

Start
1215
Environmental Sensor Adjustments
& Noise Extractor Flowchart 710
Environmental Sensors and Reference Signals Processing
and Negative Loop Feedback Processing
1220
1225
Loop
Balance
Mode?
True
False
Loop Balance
1230
Loop
Comparisons
1235
Noise
Processor
1245
Exit
1250

FIG. 12

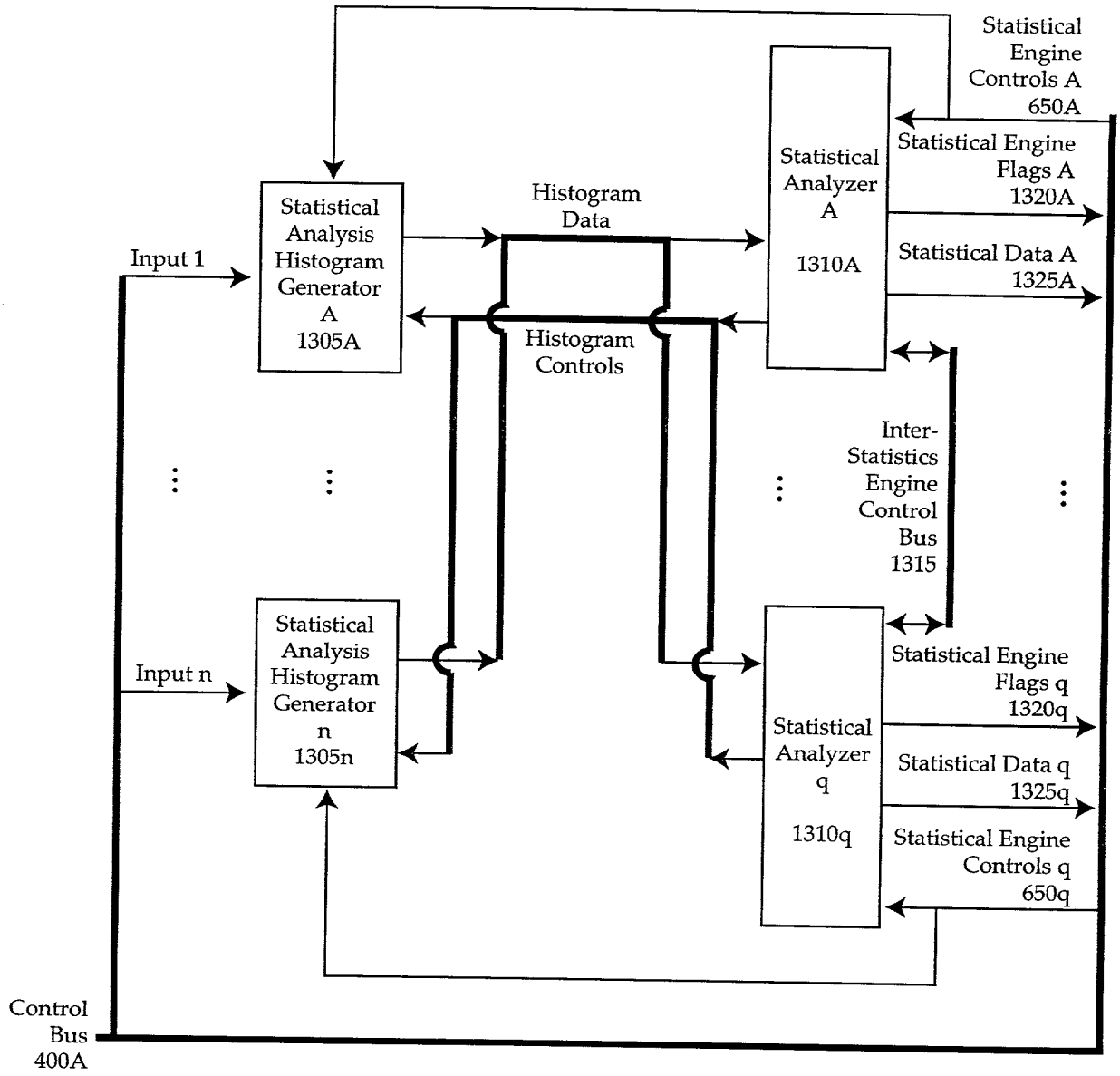

Statistical Engine Controls A 650A
Statistical Analyzer A 1310A
Statistical Engine Flags A 1320A
Statistical Data A 1325A
Statistical Analysis Histogram Generator A 1305A
Histogram Data
Input 1
Histogram Controls
Inter-Statistics Engine Control Bus 1315
Statistical Analysis Histogram Generator n 1305n
Input n
Statistical Analyzer q 1310q
Statistical Engine Flags q 1320q
Statistical Data q 1325q
Statistical Engine Controls q 650q
Control Bus 400A

FIG. 13

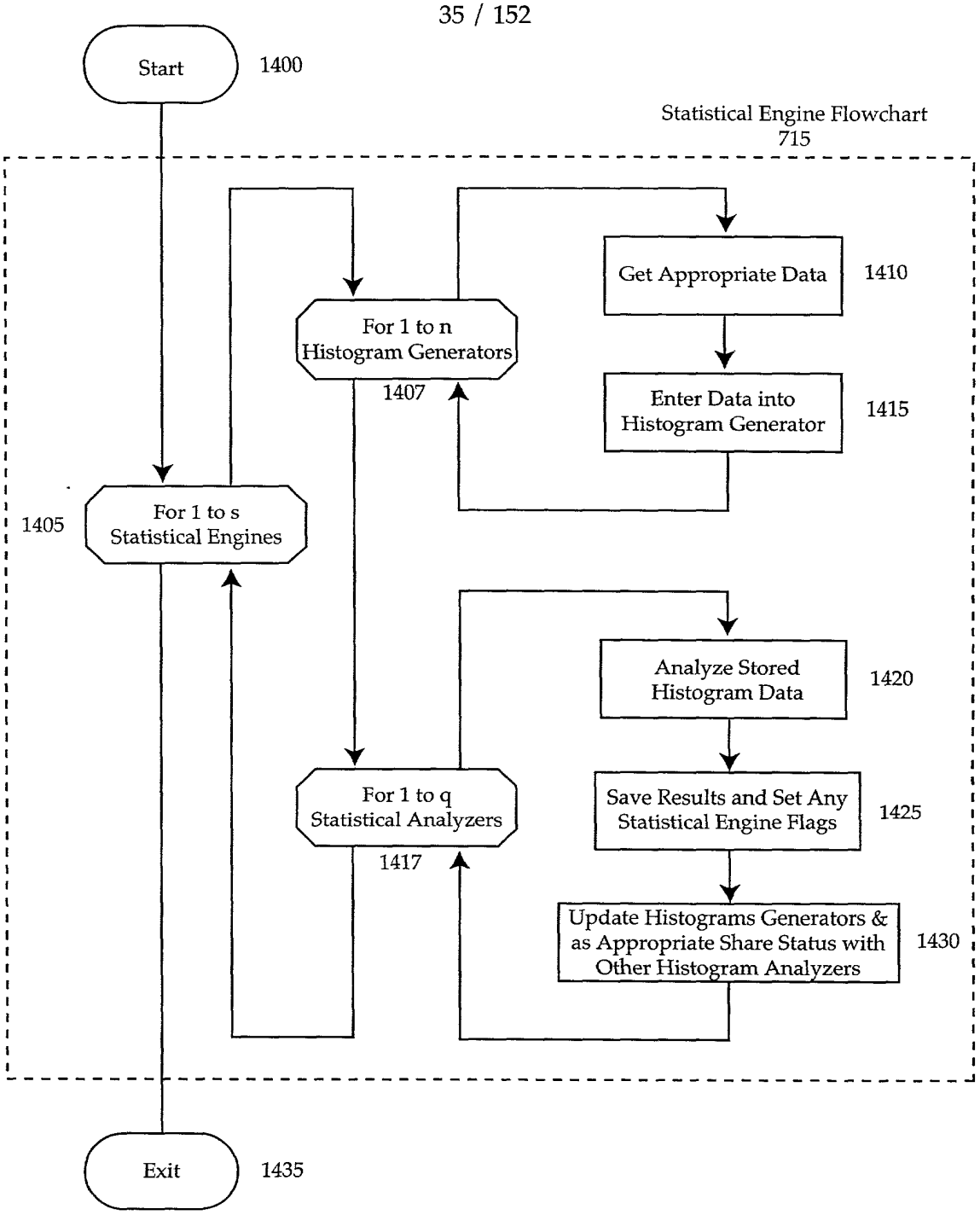

Start
1400
Statistical Engine Flowchart
715
Get Appropriate Data
1410
For 1 to n
Histogram Generators
1407
Enter Data into
Histogram Generator
1415
1405
For 1 to s
Statistical Engines
Analyze Stored
Histogram Data
1420
For 1 to q
Statistical Analyzers
1417
Save Results and Set Any
Statistical Engine Flags
1425
Update Histograms Generators &
as Appropriate Share Status with
Other Histogram Analyzers
1430
Exit
1435

FIG. 14

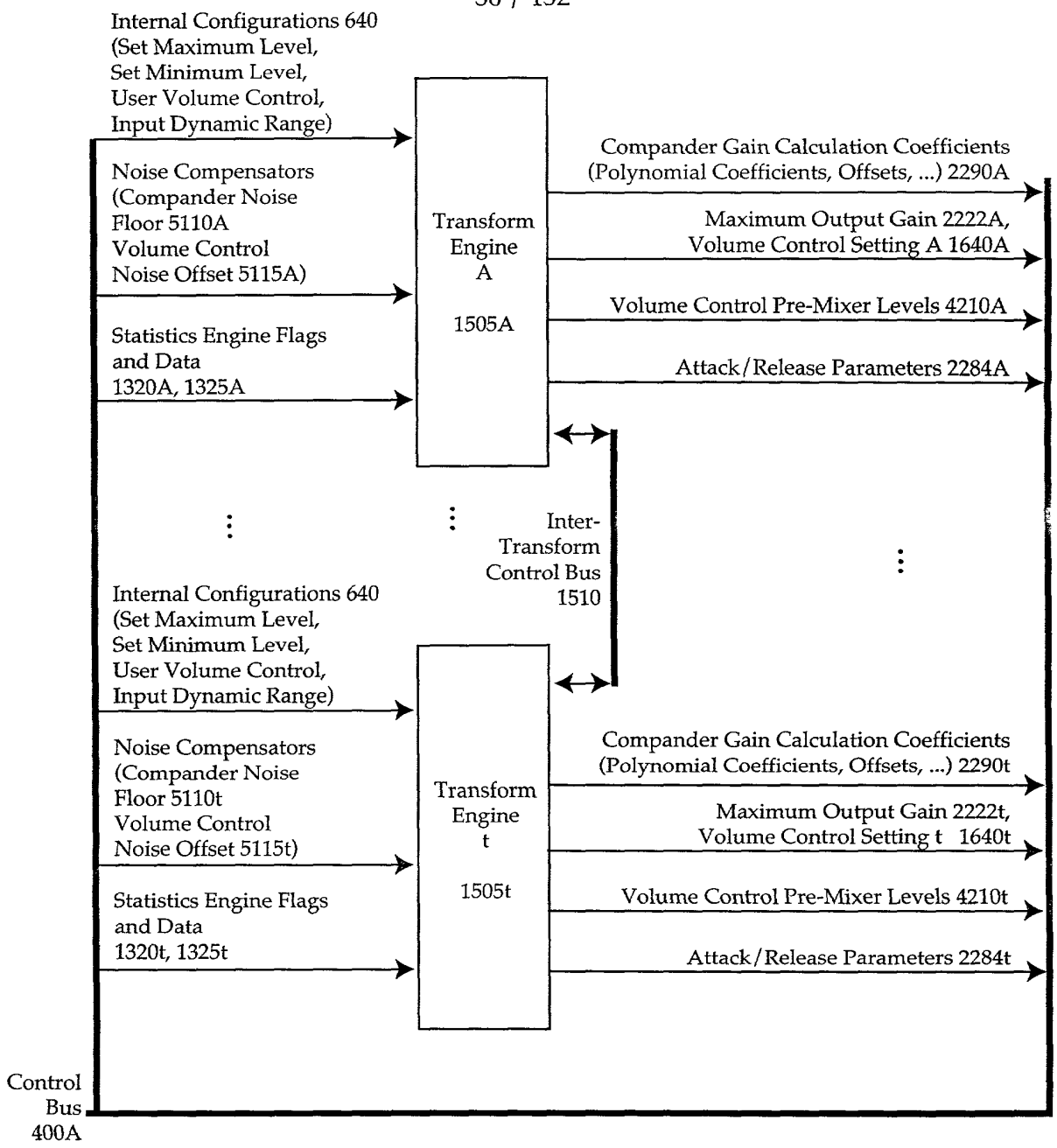

Internal Configurations 640
(Set Maximum Level,
Set Minimum Level,
User Volume Control,
Input Dynamic Range)
Noise Compensators
(Compander Noise
Floor 5110A
Volume Control
Noise Offset 5115A)
Statistics Engine Flags
and Data
1320A, 1325A
Transform
Engine
A
1505A
Compander Gain Calculation Coefficients
(Polynomial Coefficients, Offsets, ...) 2290A
Maximum Output Gain 2222A,
Volume Control Setting A 1640A
Volume Control Pre-Mixer Levels 4210A
Attack/Release Parameters 2284A
Inter-
Transform
Control Bus
1510
Internal Configurations 640
(Set Maximum Level,
Set Minimum Level,
User Volume Control,
Input Dynamic Range)
Noise Compensators
(Compander Noise
Floor 5110t
Volume Control
Noise Offset 5115t)
Statistics Engine Flags
and Data
1320t, 1325t
Transform
Engine
t
1505t
Compander Gain Calculation Coefficients
(Polynomial Coefficients, Offsets, ...) 2290t
Maximum Output Gain 2222t,
Volume Control Setting t 1640t
Volume Control Pre-Mixer Levels 4210t
Attack/Release Parameters 2284t
Control
Bus
400A

FIG. 15

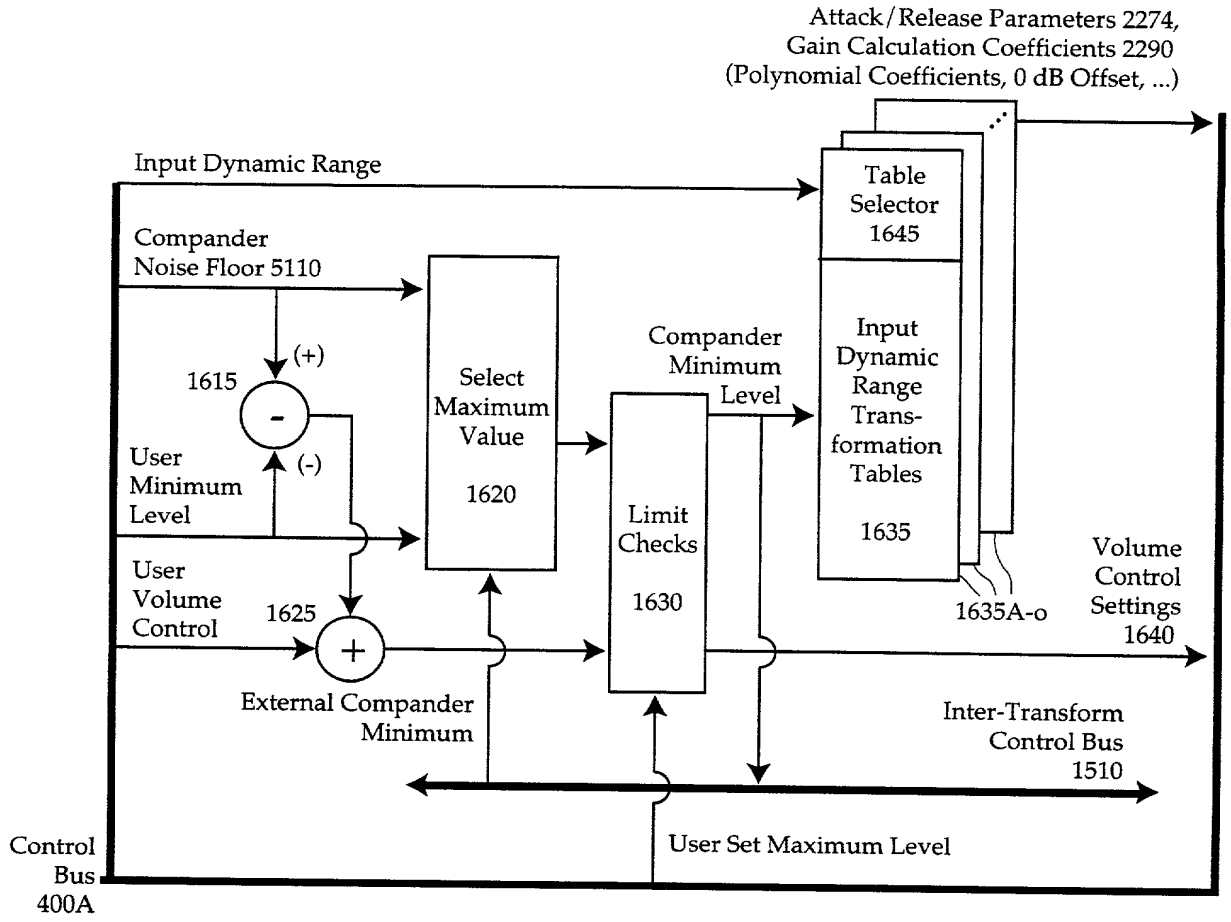

Attack/Release Parameters 2274,
Gain Calculation Coefficients 2290
(Polynomial Coefficients, 0 dB Offset, ...)
Input Dynamic Range
Table Selector 1645
Compander Noise Floor 5110
(+)
1615
(-)
User Minimum Level
Select Maximum Value 1620
Compander Minimum Level
Input Dynamic Range Trans-formation Tables 1635
Limit Checks 1630
1635A-o
Volume Control Settings 1640
User Volume Control
1625
External Compander Minimum
Inter-Transform Control Bus 1510
Control Bus 400A
User Set Maximum Level

FIG. 16

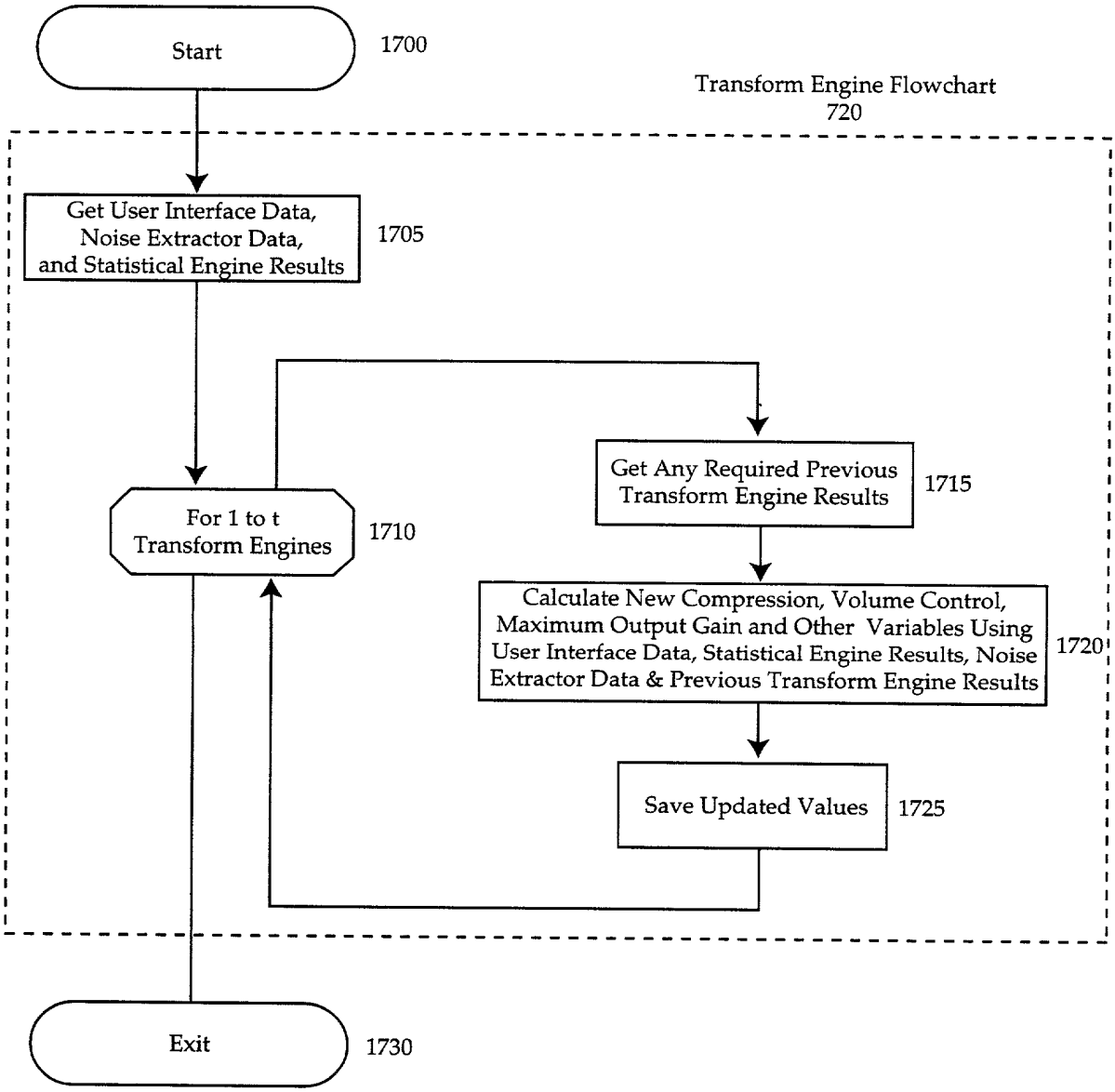

Start
1700
Transform Engine Flowchart
720
Get User Interface Data,
Noise Extractor Data,
and Statistical Engine Results
1705
Get Any Required Previous
Transform Engine Results
1715
For 1 to t
Transform Engines
1710
Calculate New Compression, Volume Control,
Maximum Output Gain and Other Variables Using
User Interface Data, Statistical Engine Results, Noise
Extractor Data & Previous Transform Engine Results
1720
Save Updated Values
1725
Exit
1730

FIG. 17

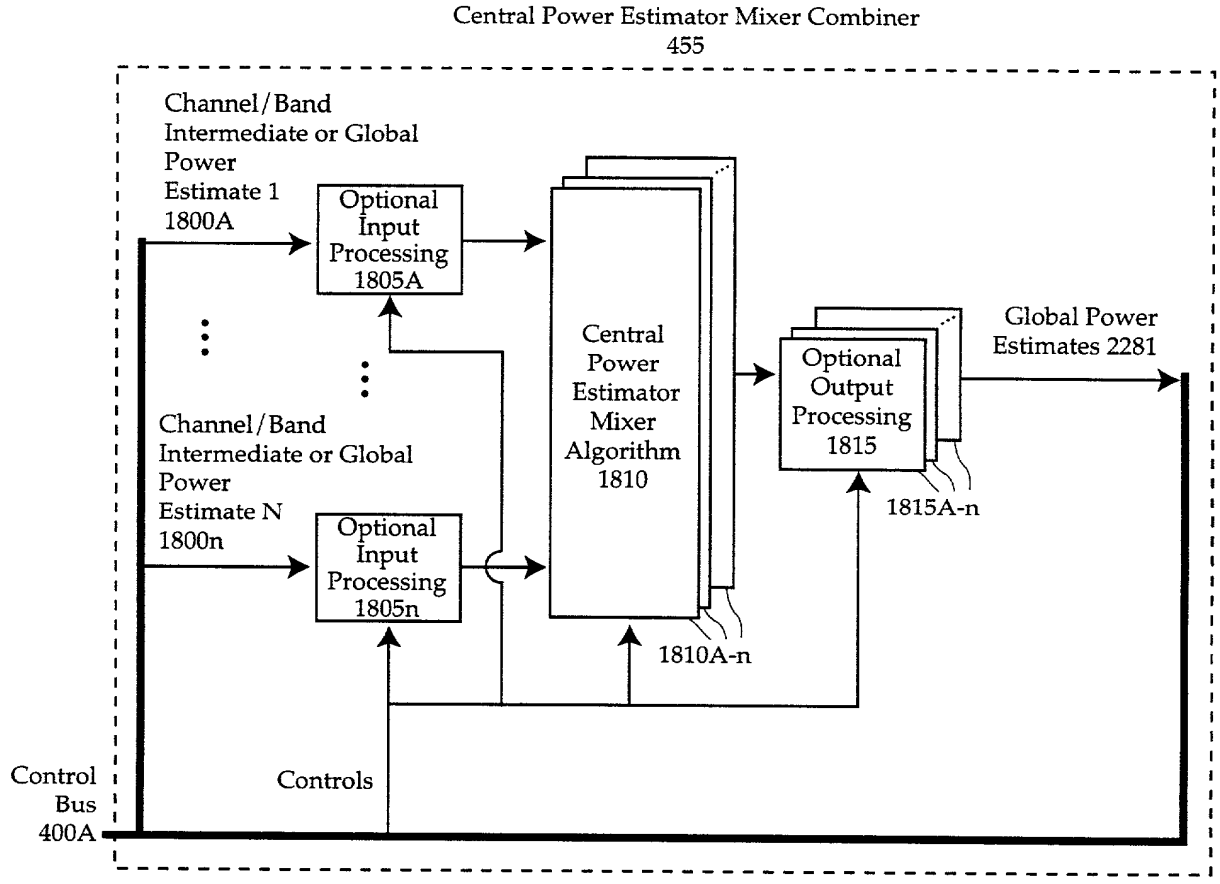

Central Power Estimator Mixer Combiner
455
Channel/Band
Intermediate or Global
Power
Estimate 1
1800A
Optional
Input
Processing
1805A
Channel/Band
Intermediate or Global
Power
Estimate N
1800n
Optional
Input
Processing
1805n
Central
Power
Estimator
Mixer
Algorithm
1810
1810A-n
Optional
Output
Processing
1815
1815A-n
Global Power
Estimates 2281
Control
Bus
400A
Controls

FIG. 18

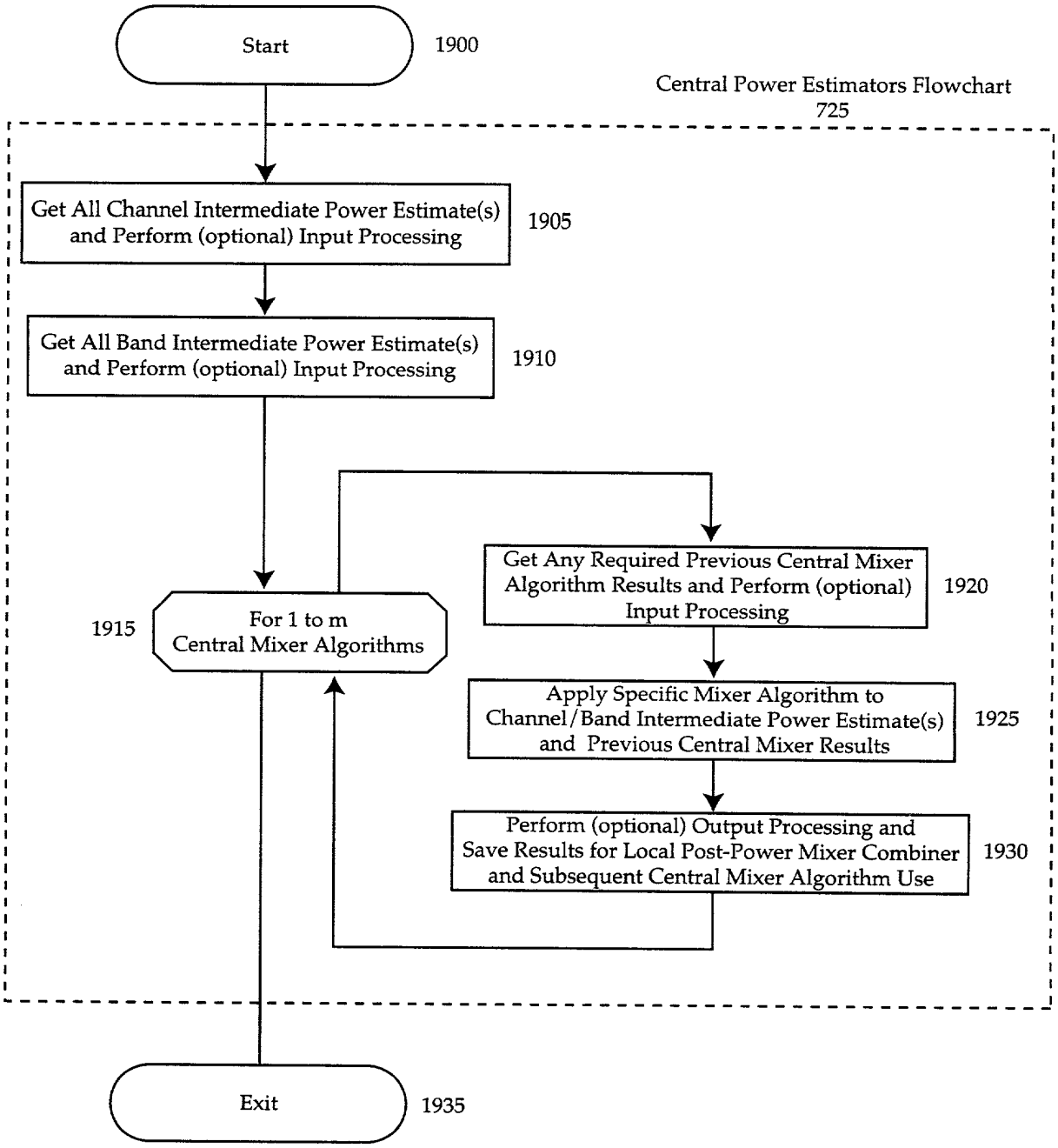

Start
1900
Central Power Estimators Flowchart
725
Get All Channel Intermediate Power Estimate(s) and Perform (optional) Input Processing
1905
Get All Band Intermediate Power Estimate(s) and Perform (optional) Input Processing
1910
1915
For 1 to m Central Mixer Algorithms
Get Any Required Previous Central Mixer Algorithm Results and Perform (optional) Input Processing
1920
Apply Specific Mixer Algorithm to Channel/Band Intermediate Power Estimate(s) and Previous Central Mixer Results
1925
Perform (optional) Output Processing and Save Results for Local Post-Power Mixer Combiner and Subsequent Central Mixer Algorithm Use
1930
Exit
1935

FIG. 19

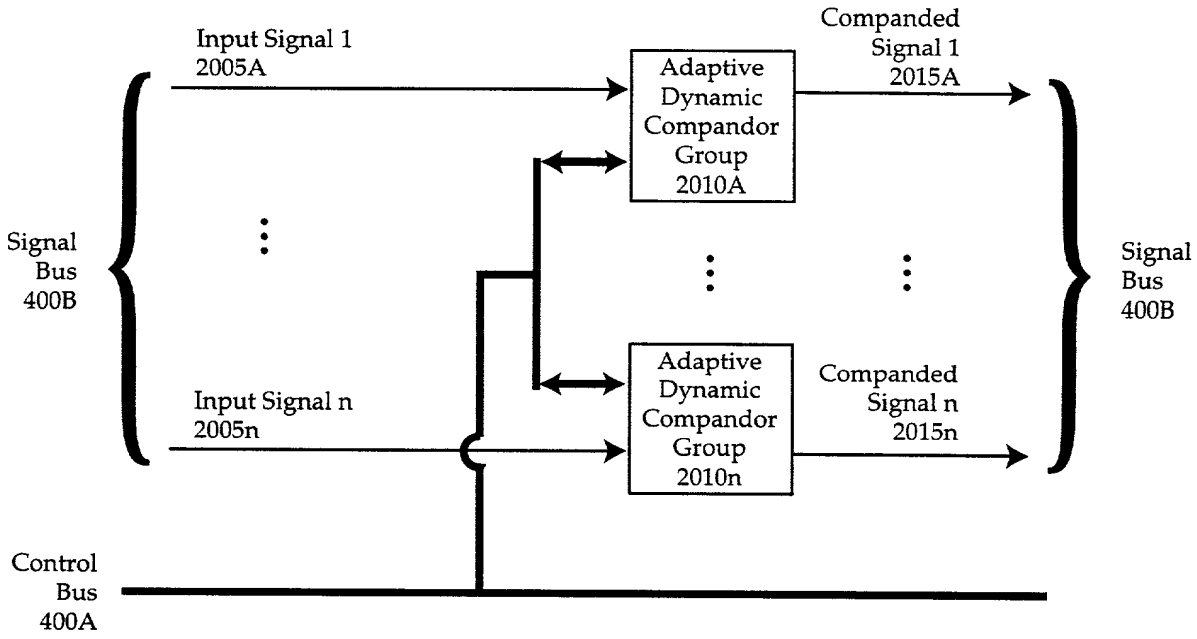

Input Signal 1
2005A
Companded
Signal 1
2015A
Adaptive
Dynamic
Compandor
Group
2010A
Signal
Bus
400B
Signal
Bus
400B
Adaptive
Dynamic
Compandor
Group
2010n
Input Signal n
2005n
Companded
Signal n
2015n
Control
Bus
400A

FIG. 20A

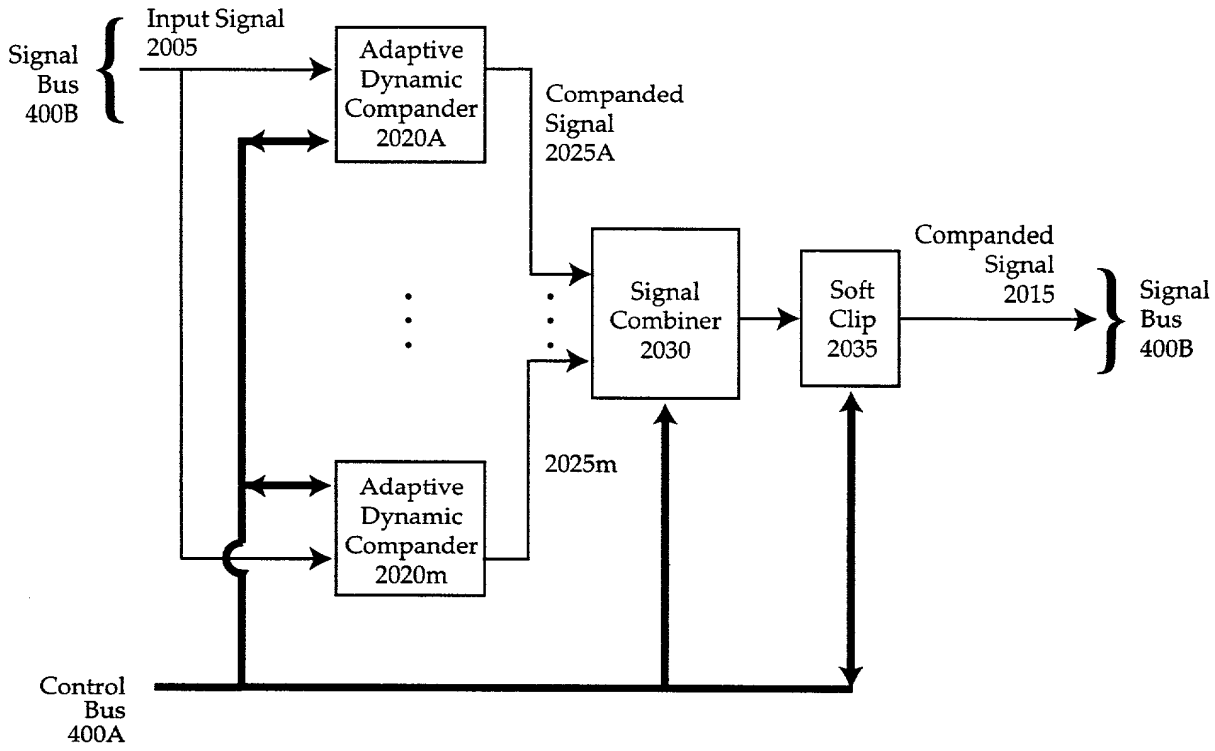

Signal Bus 400B
Input Signal 2005
Adaptive Dynamic Compander 2020A
Companded Signal 2025A
Signal Combiner 2030
Soft Clip 2035
Companded Signal 2015
Signal Bus 400B
Adaptive Dynamic Compander 2020m
2025m
Control Bus 400A

FIG. 20B

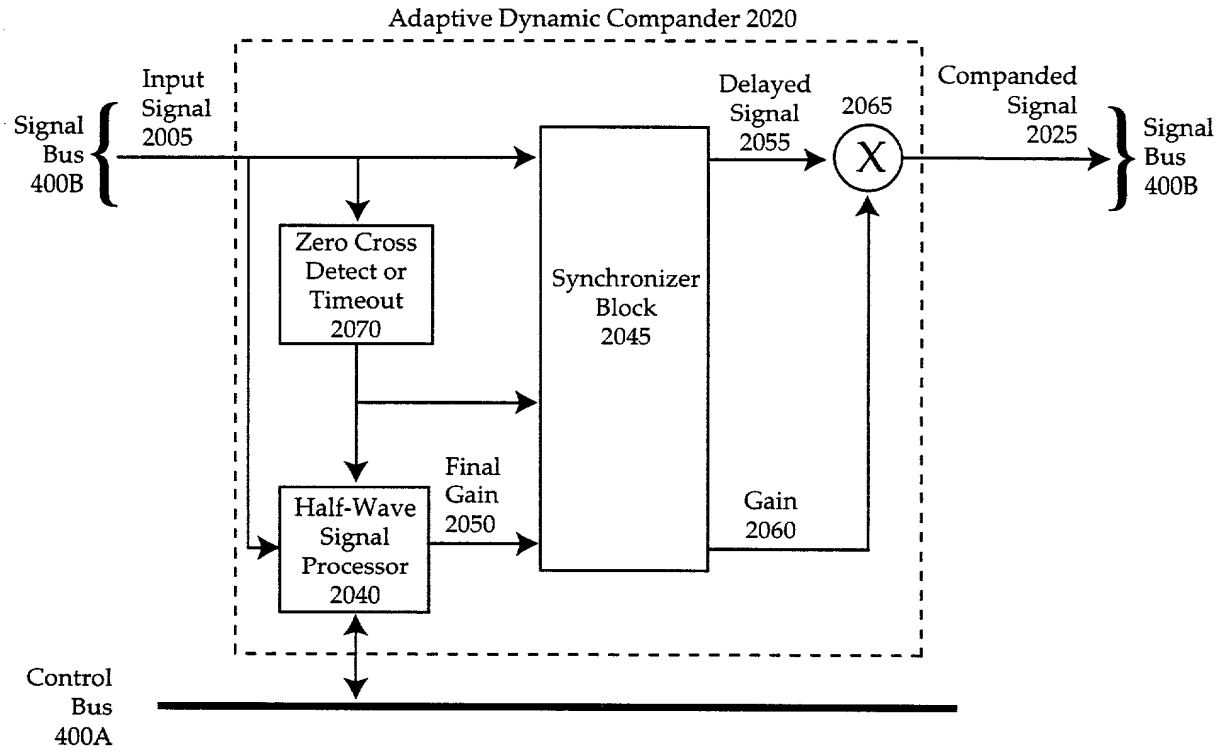

Adaptive Dynamic Compander 2020
Signal Bus 400B
Input Signal 2005
Zero Cross Detect or Timeout 2070
Half-Wave Signal Processor 2040
Final Gain 2050
Synchronizer Block 2045
Delayed Signal 2055
2065
X
Gain 2060
Companded Signal 2025
Signal Bus 400B
Control Bus 400A

FIG. 20C

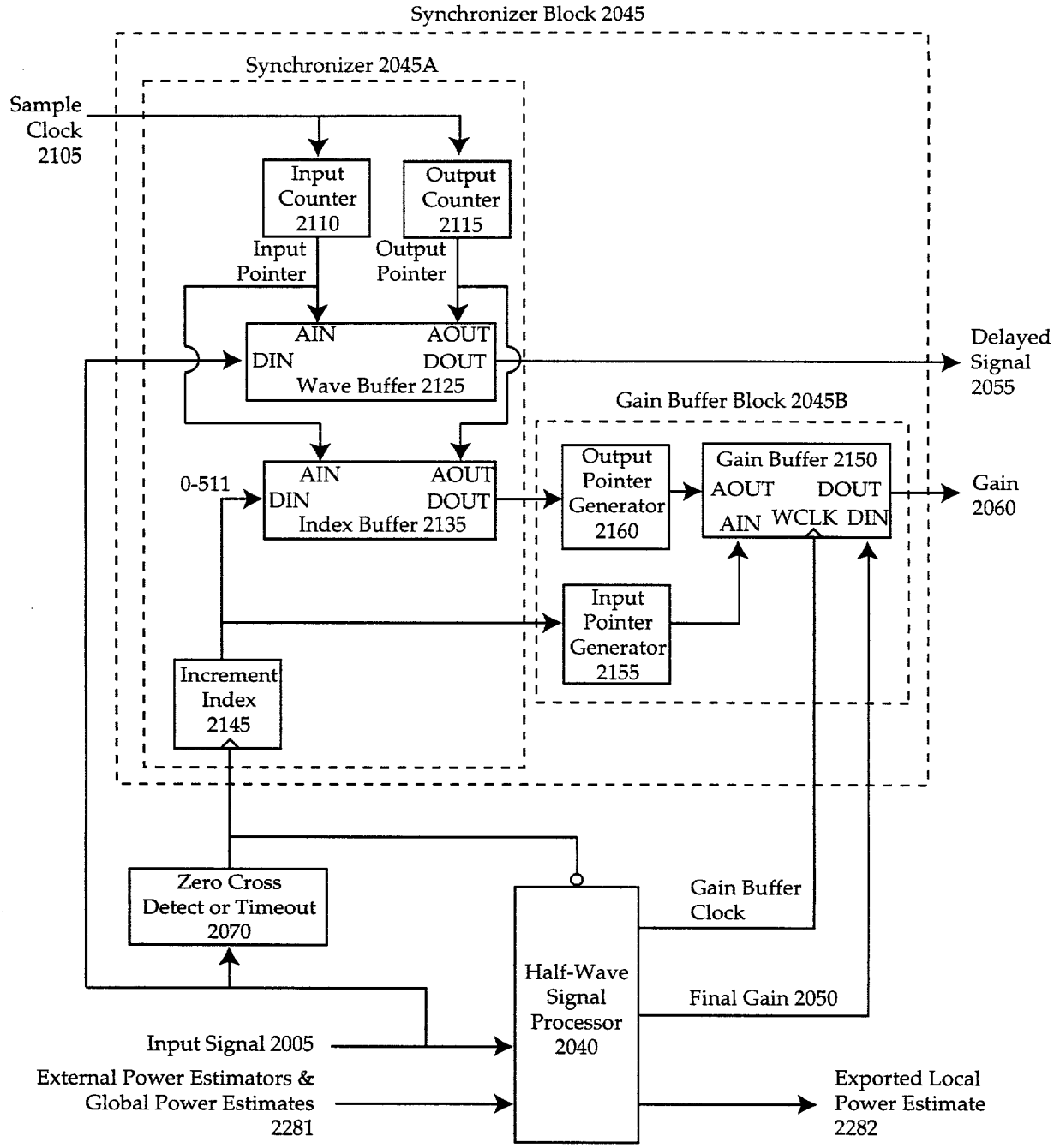

Synchronizer Block 2045
Synchronizer 2045A
Sample Clock 2105
Input Counter 2110
Output Counter 2115
Input Pointer
Output Pointer
AIN
DIN
AOUT
DOUT
Wave Buffer 2125
Delayed Signal 2055
Gain Buffer Block 2045B
0-511
Index Buffer 2135
Output Pointer Generator 2160
Gain Buffer 2150
AOUT
DOUT
AIN
WCLK
DIN
Gain 2060
Input Pointer Generator 2155
Increment Index 2145
Zero Cross Detect or Timeout 2070
Gain Buffer Clock
Half-Wave Signal Processor 2040
Final Gain 2050
Input Signal 2005
External Power Estimators & Global Power Estimates 2281
Exported Local Power Estimate 2282

FIG. 21A

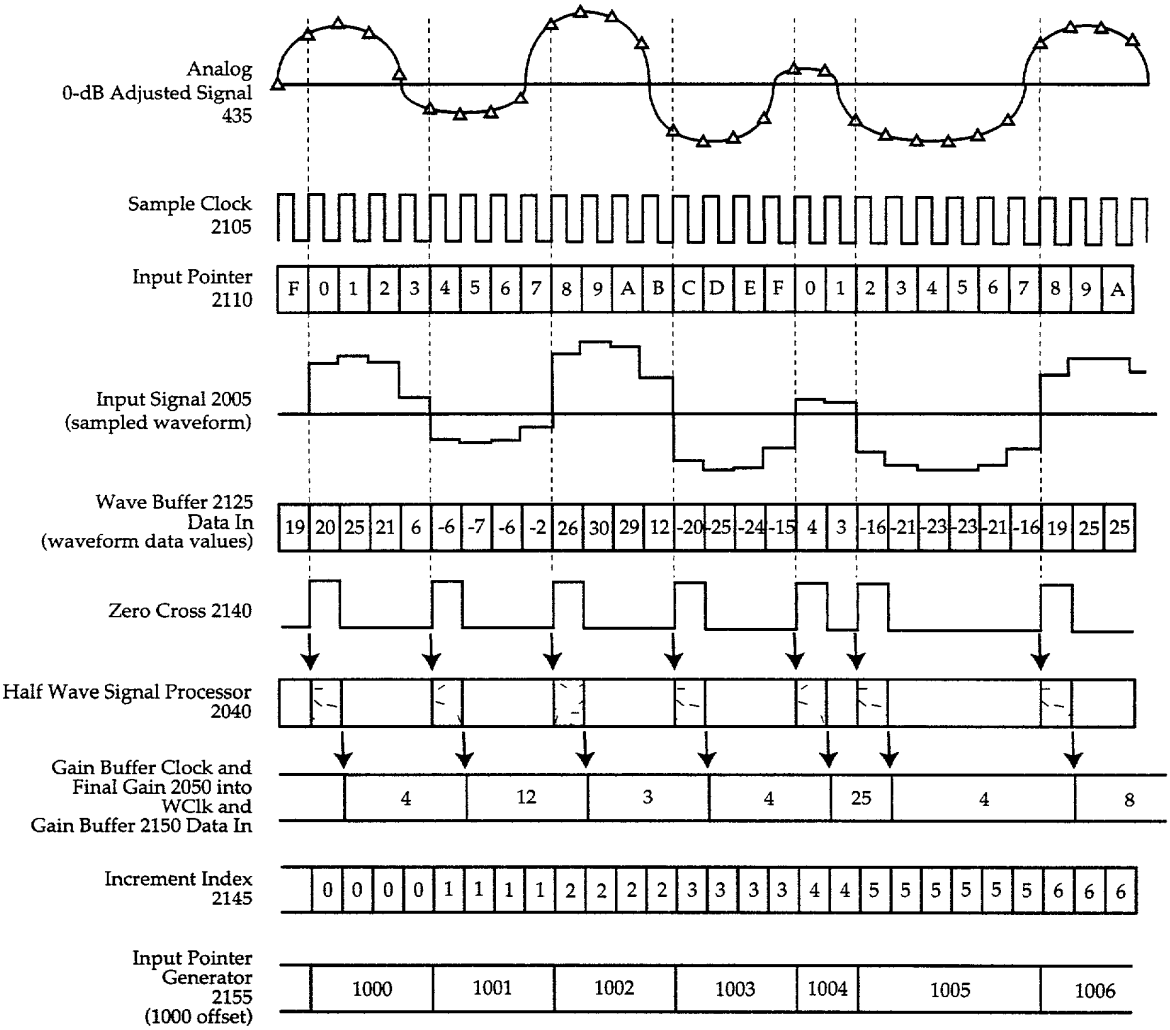

Analog
0-dB Adjusted Signal
435
Sample Clock
2105
Input Pointer
2110
F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A
Input Signal 2005
(sampled waveform)
Wave Buffer 2125
Data In
(waveform data values)
19 20 25 21 6 -6 -7 -6 -2 26 30 29 12 -20 -25 -24 -15 4 3 -16 -21 -23 -23 -21 -16 19 25 25
Zero Cross 2140
Half Wave Signal Processor
2040
Gain Buffer Clock and
Final Gain 2050 into
WClk and
Gain Buffer 2150 Data In
4 12 3 4 25 4 8
Increment Index
2145
0 0 0 0 1 1 1 1 2 2 2 2 3 3 3 3 4 4 5 5 5 5 5 5 6 6 6
Input Pointer
Generator
2155
(1000 offset)
1000 1001 1002 1003 1004 1005 1006

FIG. 21B

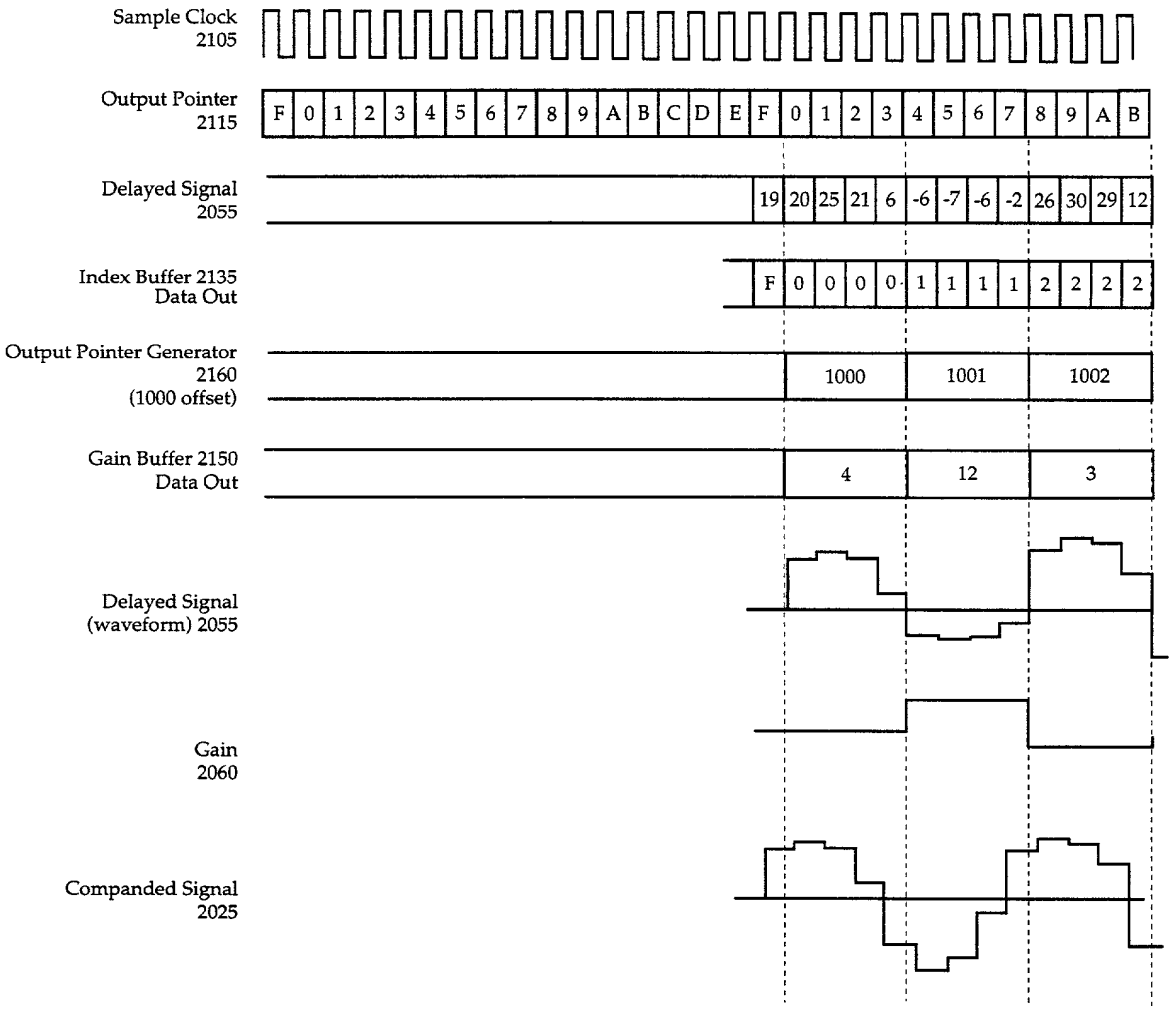

Sample Clock 2105
Output Pointer 2115
F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B
Delayed Signal 2055
19 20 25 21 6 -6 -7 -6 -2 26 30 29 12
Index Buffer 2135 Data Out
F 0 0 0 0 1 1 1 1 2 2 2 2
Output Pointer Generator 2160 (1000 offset)
1000
1001
1002
Gain Buffer 2150 Data Out
4
12
3
Delayed Signal (waveform) 2055
Gain 2060
Companded Signal 2025

FIG. 21C

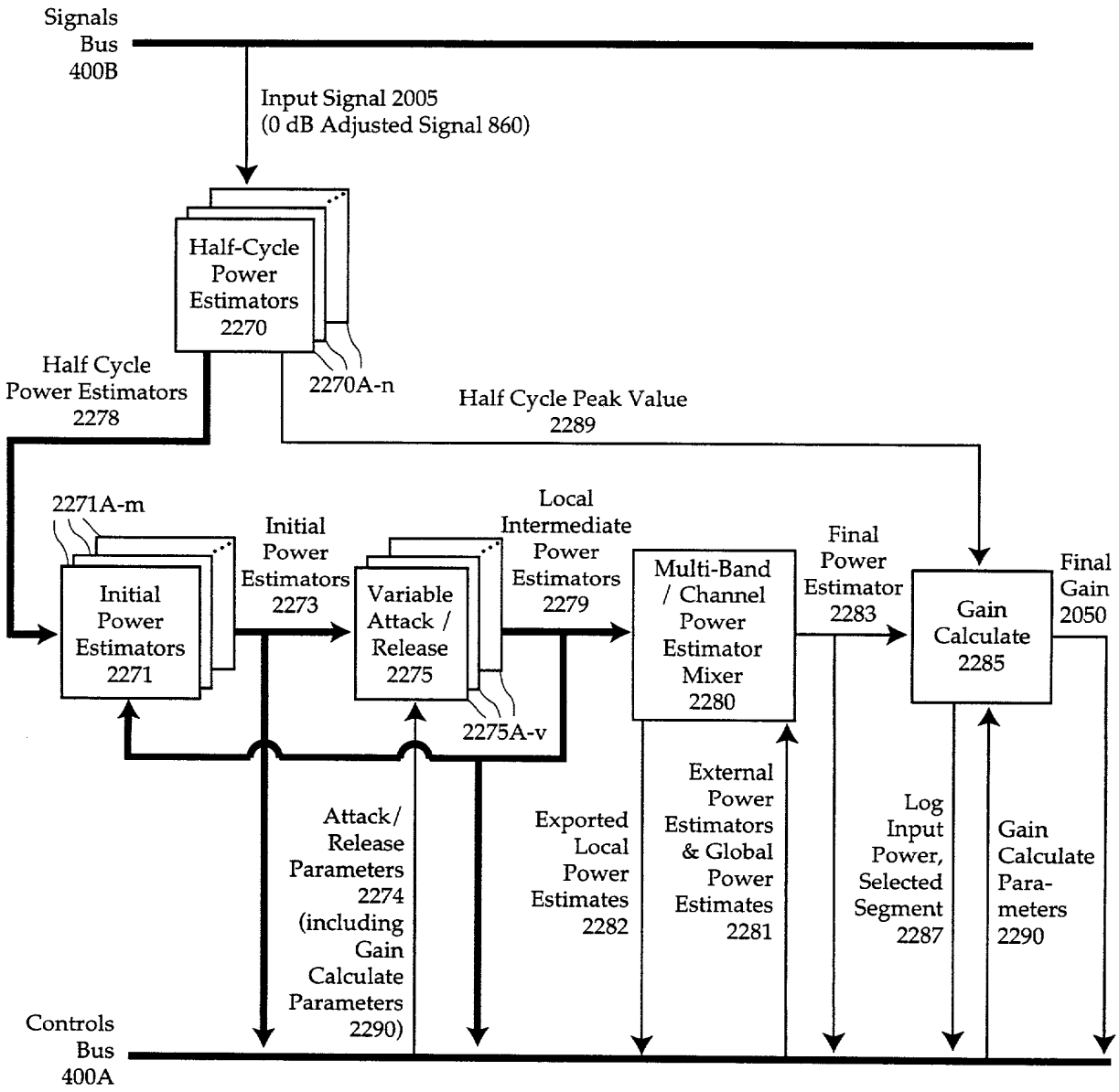

Signals Bus 400B
Input Signal 2005 (0 dB Adjusted Signal 860)
Half-Cycle Power Estimators 2270
2270A-n
Half Cycle Power Estimators 2278
Half Cycle Peak Value 2289
2271A-m
Initial Power Estimators 2271
Initial Power Estimators 2273
Variable Attack / Release 2275
2275A-v
Local Intermediate Power Estimators 2279
Multi-Band / Channel Power Estimator Mixer 2280
Final Power Estimator 2283
Gain Calculate 2285
Final Gain 2050
Attack/ Release Parameters 2274 (including Gain Calculate Parameters 2290)
Exported Local Power Estimates 2282
External Power Estimators & Global Power Estimates 2281
Log Input Power, Selected Segment 2287
Gain Calculate Para-meters 2290
Controls Bus 400A

FIG. 22

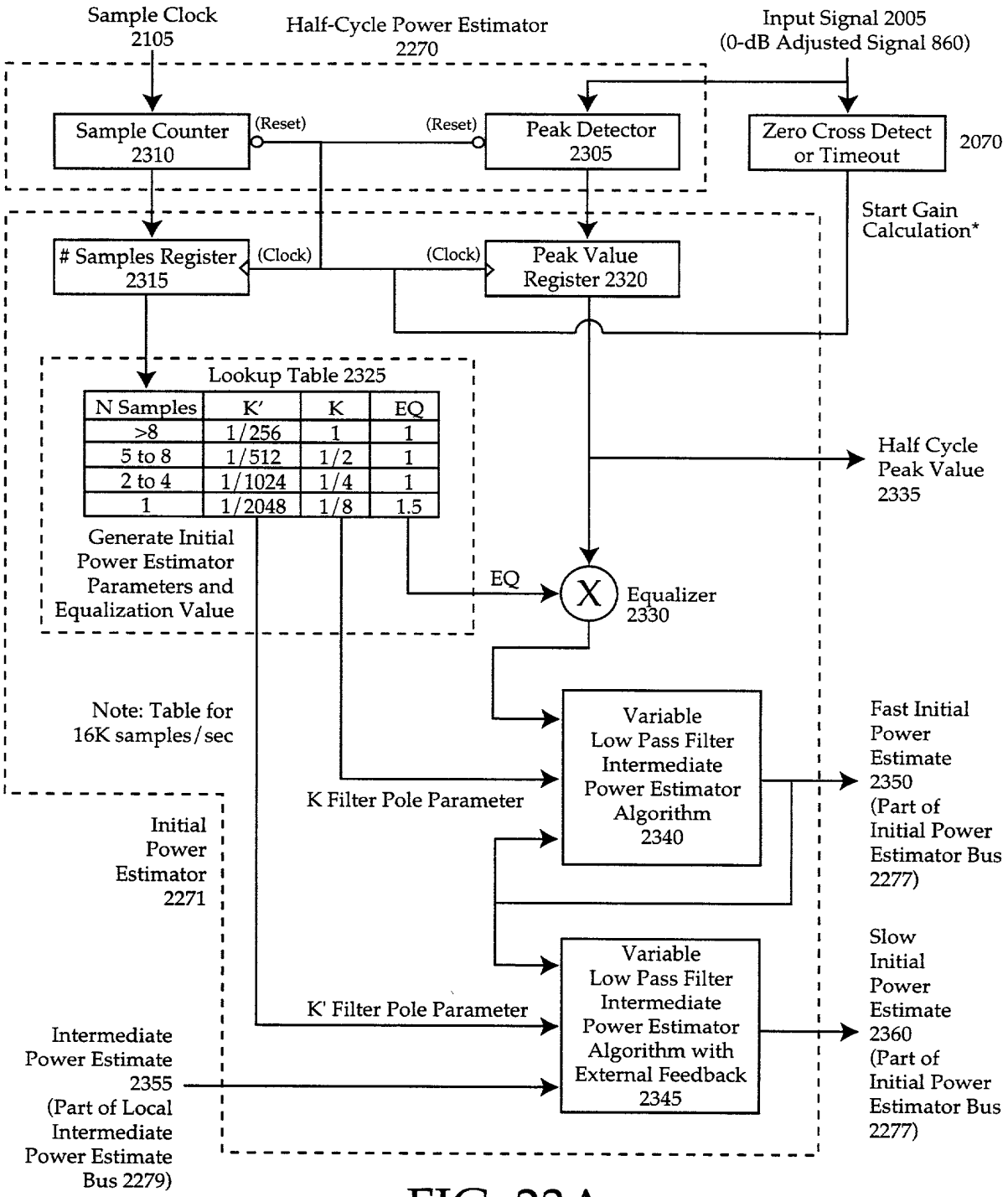

Sample Clock 2105
Half-Cycle Power Estimator 2270
Input Signal 2005 (0-dB Adjusted Signal 860)
Sample Counter 2310
(Reset)
(Reset)
Peak Detector 2305
Zero Cross Detect or Timeout
2070
Start Gain Calculation*
Samples Register 2315
(Clock)
(Clock)
Peak Value Register 2320
Lookup Table 2325
N Samples | K' | K | EQ
>8 | 1/256 | 1 | 1
5 to 8 | 1/512 | 1/2 | 1
2 to 4 | 1/1024 | 1/4 | 1
1 | 1/2048 | 1/8 | 1.5
Half Cycle Peak Value 2335
Generate Initial Power Estimator Parameters and Equalization Value
EQ
X
Equalizer 2330
Note: Table for 16K samples/sec
Variable Low Pass Filter Intermediate Power Estimator Algorithm 2340
Fast Initial Power Estimate 2350 (Part of Initial Power Estimator Bus 2277)
K Filter Pole Parameter
Initial Power Estimator 2271
K' Filter Pole Parameter
Variable Low Pass Filter Intermediate Power Estimator Algorithm with External Feedback 2345
Slow Initial Power Estimate 2360 (Part of Initial Power Estimator Bus 2277)
Intermediate Power Estimate 2355 (Part of Local Intermediate Power Estimate Bus 2279)

FIG. 23A

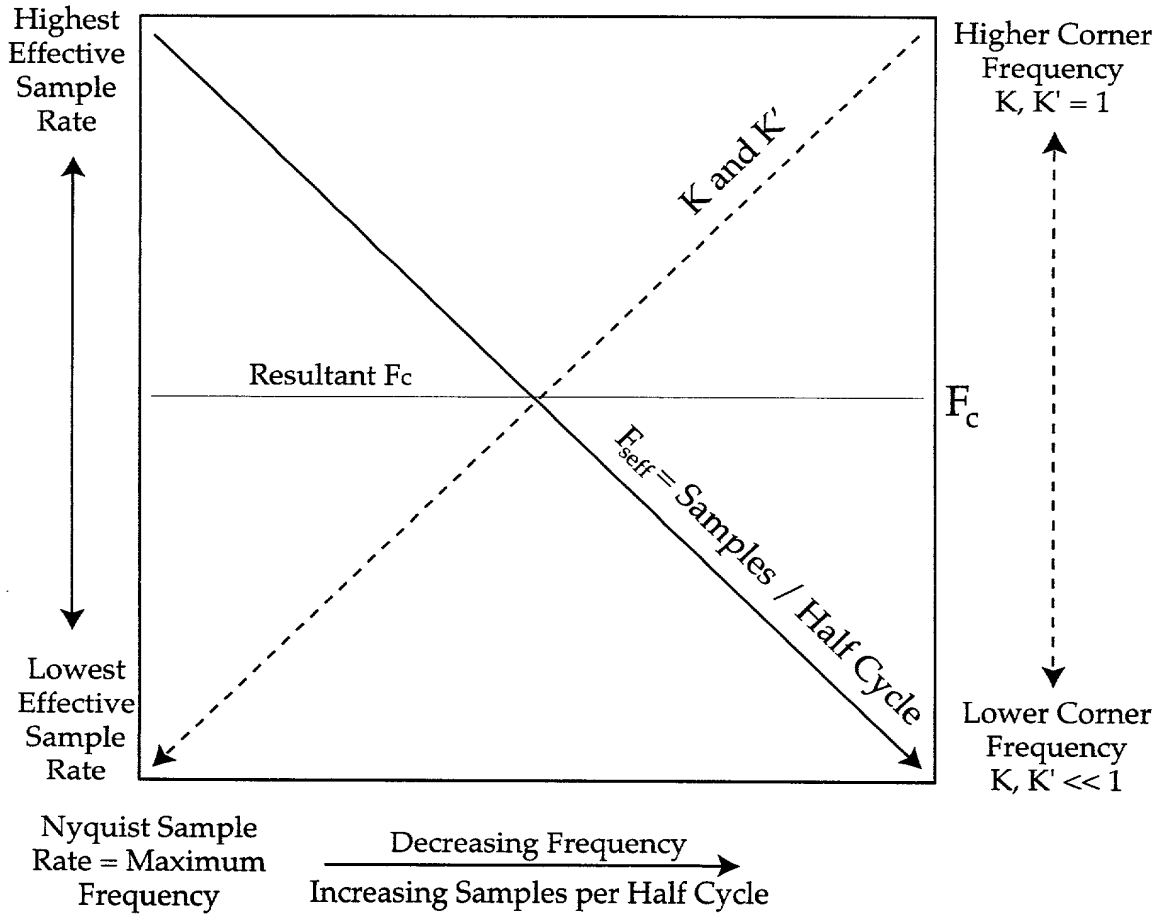

Highest Effective Sample Rate
Lowest Effective Sample Rate
Nyquist Sample Rate = Maximum Frequency
Resultant Fc
K and K'
Fseff = Samples / Half Cycle
Higher Corner Frequency K, K' = 1
Fc
Lower Corner Frequency K, K' << 1
Decreasing Frequency
Increasing Samples per Half Cycle

FIG. 23B

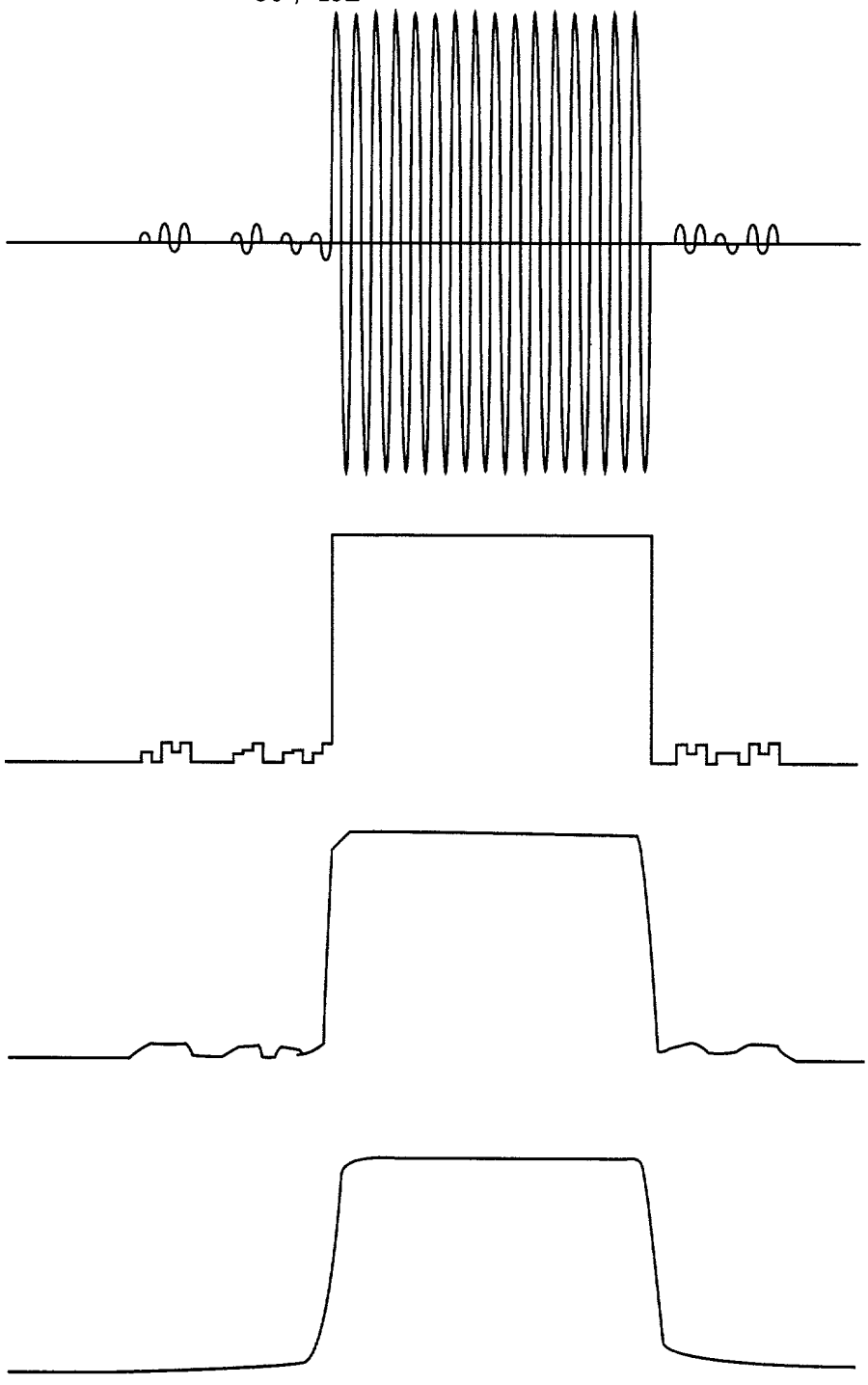

Input Signal
2005
(0-dB Adjusted
Signal 860)
Half Cycle
Peak Value
2289
Fast Initial
Power Estimate
2350
Intermediate
Power
Estimate
2355

FIG. 23C

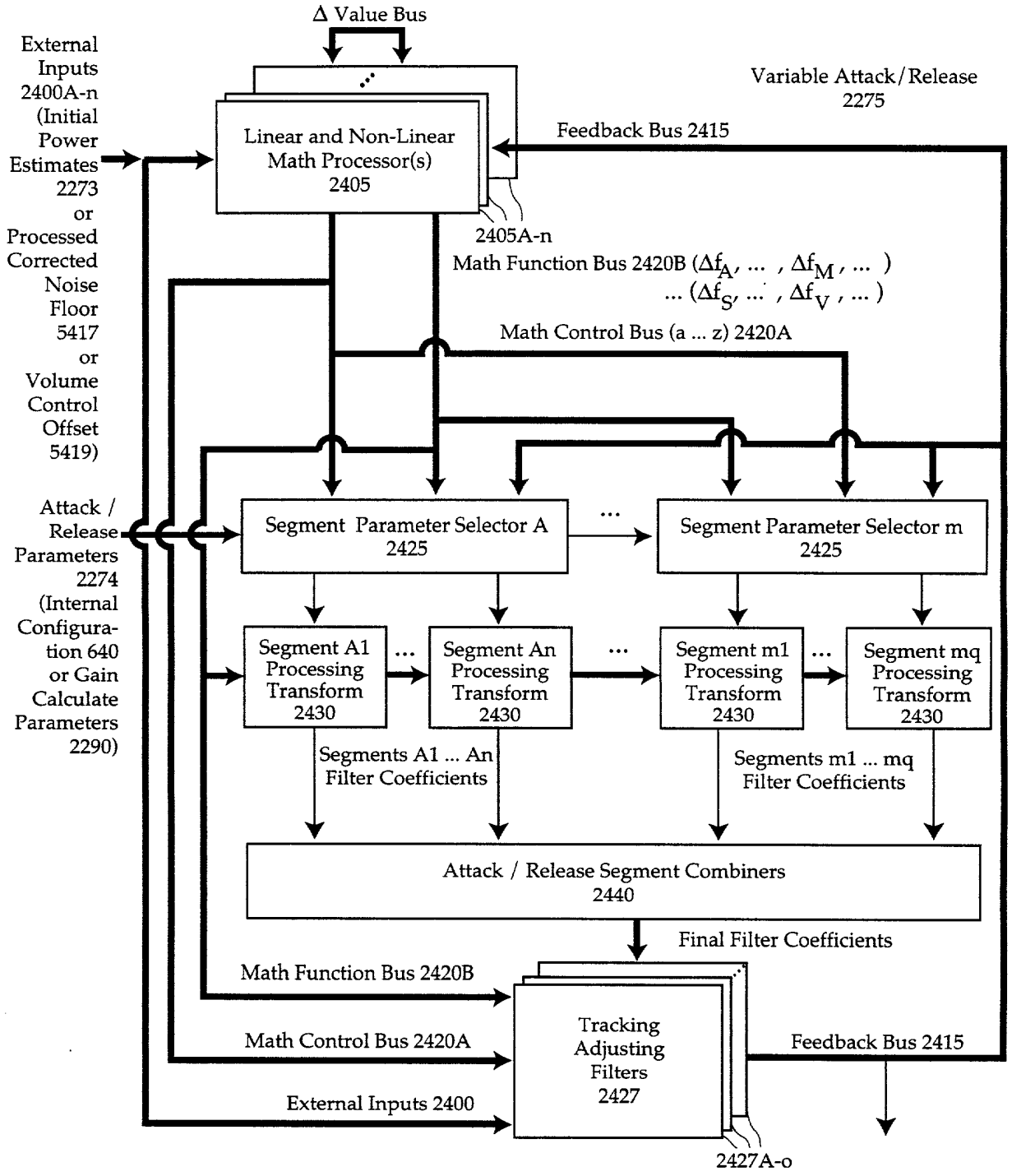

Δ Value Bus
External Inputs 2400A-n (Initial Power Estimates 2273 or Processed Corrected Noise Floor 5417 or Volume Control Offset 5419)
Linear and Non-Linear Math Processor(s) 2405
Variable Attack/Release 2275
Feedback Bus 2415
2405A-n
Math Function Bus 2420B (Δf_A, ... , Δf_M, ...) ... (Δf_S, ... , Δf_V, ...)
Math Control Bus (a ... z) 2420A
Attack / Release Parameters 2274 (Internal Configuration 640 or Gain Calculate Parameters 2290)
Segment Parameter Selector A 2425
Segment Parameter Selector m 2425
Segment A1 Processing Transform 2430
Segment An Processing Transform 2430
Segment m1 Processing Transform 2430
Segment mq Processing Transform 2430
Segments A1 ... An Filter Coefficients
Segments m1 ... mq Filter Coefficients
Attack / Release Segment Combiners 2440
Final Filter Coefficients
Math Function Bus 2420B
Math Control Bus 2420A
External Inputs 2400
Tracking Adjusting Filters 2427
Feedback Bus 2415
2427A-o
Local Intermediate Power Estimates 2279 or Long Duration Noise Floor 5425 or Long Duration Noise Offset 5427

FIG. 24A

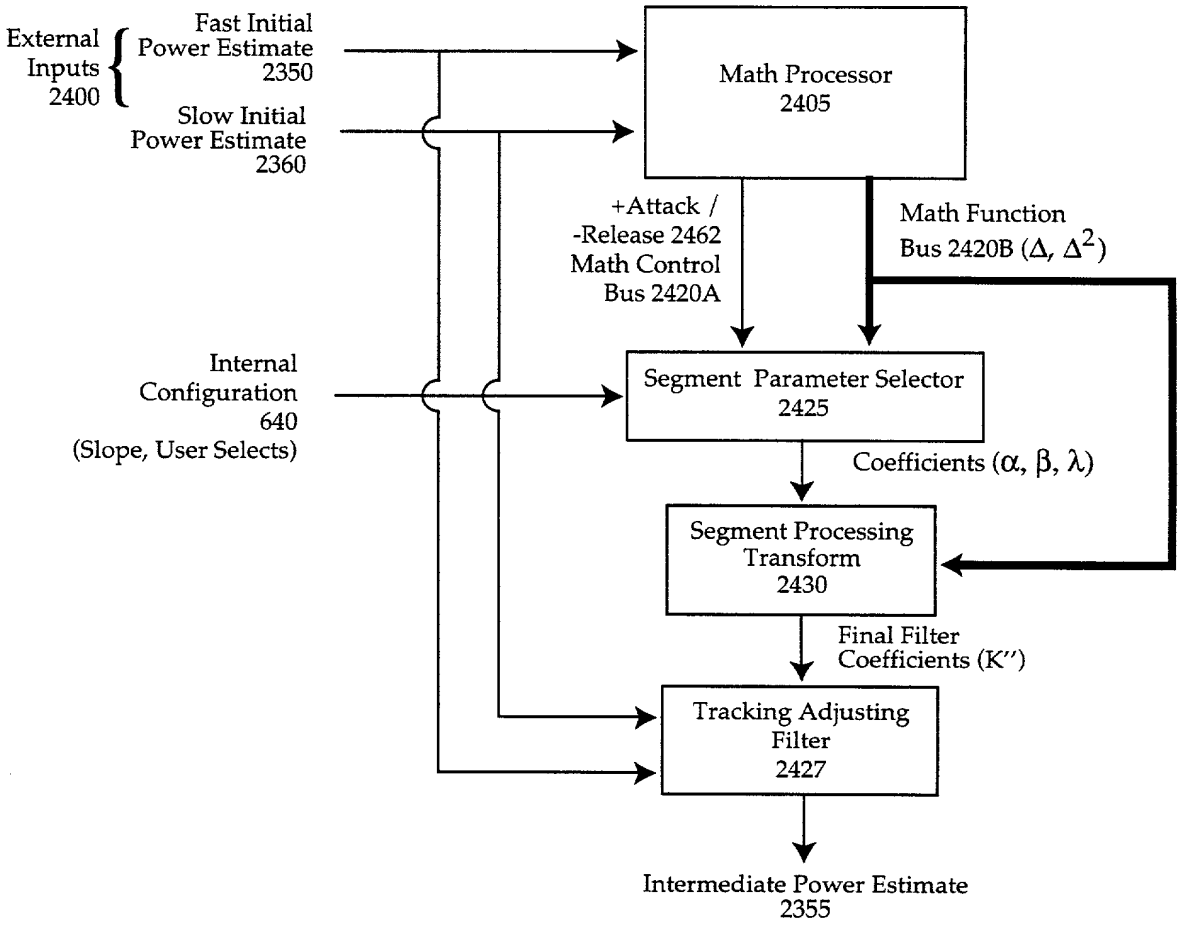

External Inputs 2400
Fast Initial Power Estimate 2350
Slow Initial Power Estimate 2360
Math Processor 2405
+Attack / -Release 2462 Math Control Bus 2420A
Math Function Bus 2420B (Δ, Δ²)
Internal Configuration 640 (Slope, User Selects)
Segment Parameter Selector 2425
Coefficients (α, β, λ)
Segment Processing Transform 2430
Final Filter Coefficients (K'')
Tracking Adjusting Filter 2427
Intermediate Power Estimate 2355

FIG. 24B

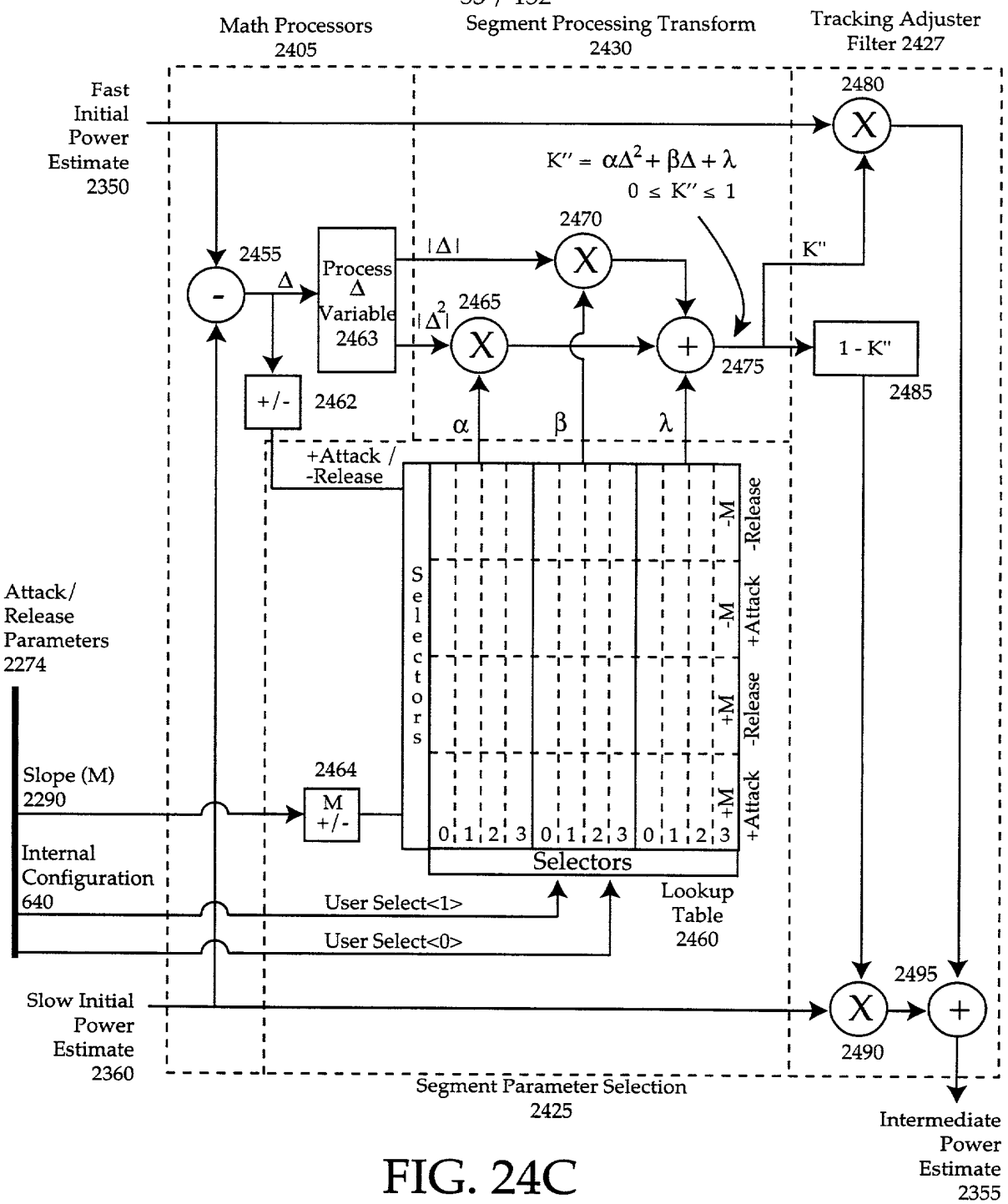

Math Processors
2405
Segment Processing Transform
2430
Tracking Adjuster
Filter 2427
Fast
Initial
Power
Estimate
2350
2480
$K'' = \alpha\Delta^2 + \beta\Delta + \lambda$
$0 \le K'' \le 1$
2470
2455
Δ
Process
Δ
Variable
2463
|Δ|
$|\Delta^2|$
2465
K"
1 - K"
2485
2475
+/-
2462
α
β
λ
+Attack /
-Release
Attack/
Release
Parameters
2274
Selectors
-M
-Release
+Attack
+M
-Release
-M
+Attack
+M
0 1 2 3 0 1 2 3 0 1 2 3
Selectors
Slope (M)
2290
2464
M
+/-
Internal
Configuration
640
User Select<1>
User Select<0>
Lookup
Table
2460
2495
Slow Initial
Power
Estimate
2360
2490
Segment Parameter Selection
2425
Intermediate
Power
Estimate
2355

FIG. 24C

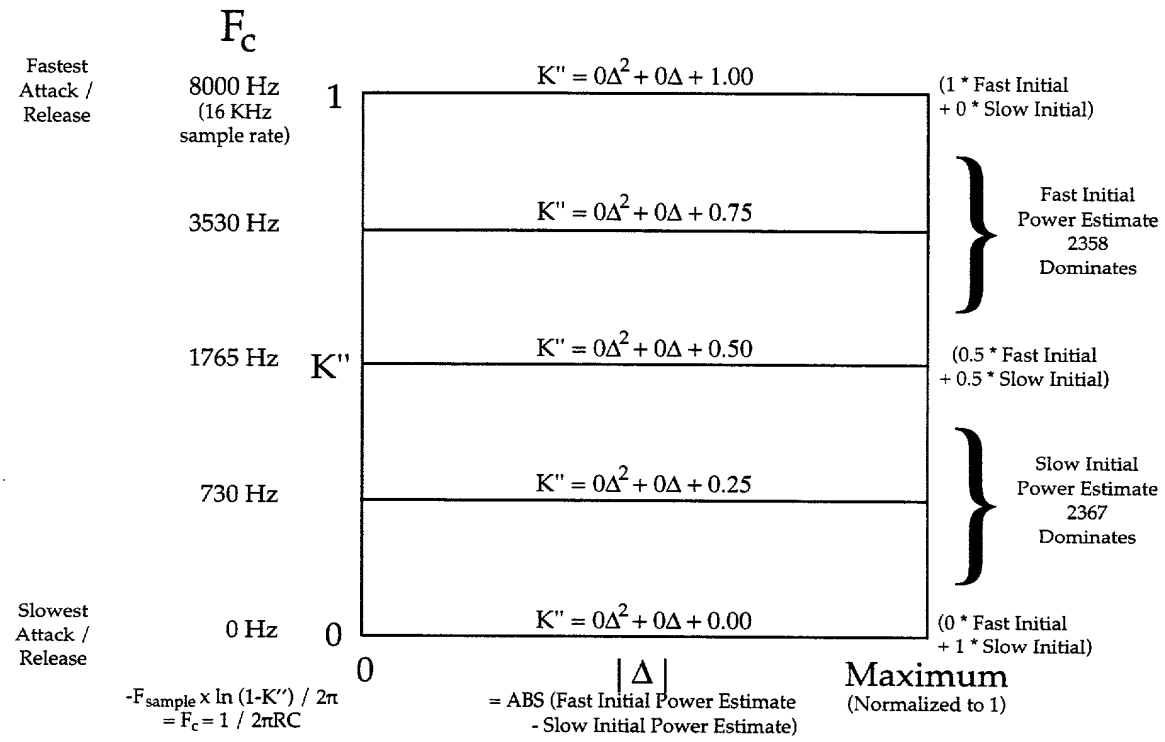

F_c
Fastest Attack / Release
8000 Hz (16 KHz sample rate)
3530 Hz
1765 Hz
730 Hz
Slowest Attack / Release
0 Hz
K"
1
0
$K" = 0\Delta^2 + 0\Delta + 1.00$
$K" = 0\Delta^2 + 0\Delta + 0.75$
$K" = 0\Delta^2 + 0\Delta + 0.50$
$K" = 0\Delta^2 + 0\Delta + 0.25$
$K" = 0\Delta^2 + 0\Delta + 0.00$
(1 * Fast Initial + 0 * Slow Initial)
Fast Initial Power Estimate 2358 Dominates
(0.5 * Fast Initial + 0.5 * Slow Initial)
Slow Initial Power Estimate 2367 Dominates
(0 * Fast Initial + 1 * Slow Initial)
0
$|\Delta|$
Maximum
(Normalized to 1)
$-F_{sample} \times \ln(1-K") / 2\pi = F_c = 1 / 2\pi RC$
= ABS (Fast Initial Power Estimate - Slow Initial Power Estimate)

FIG. 24D

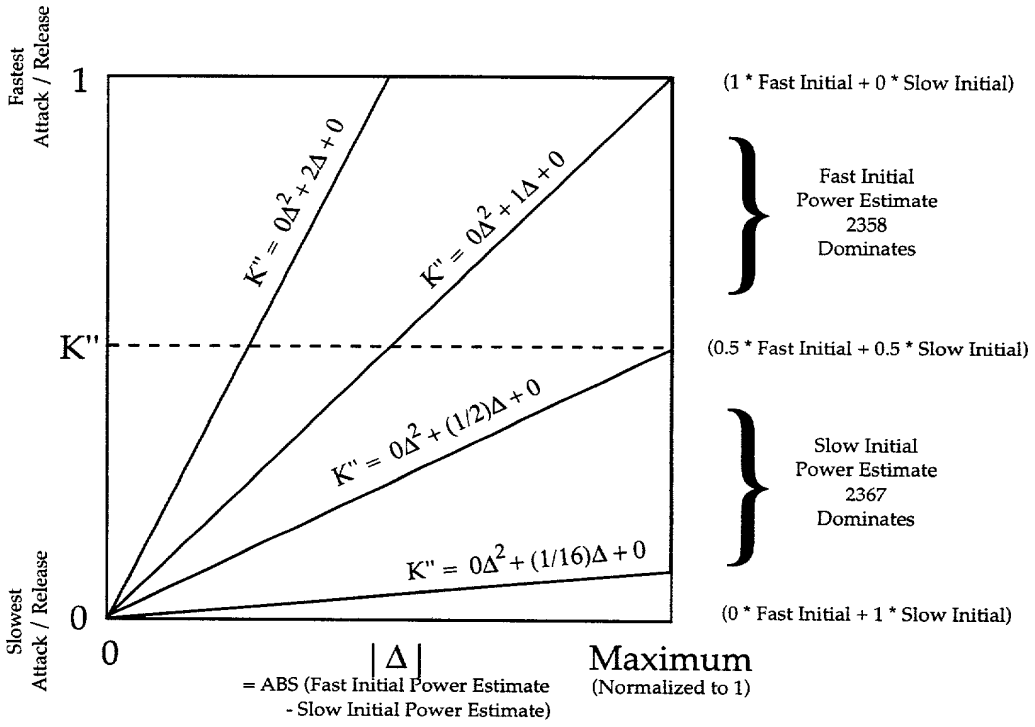

Fastest
Attack / Release
1
K"
0
Slowest
Attack / Release
$K" = 0\Delta^2 + 2\Delta + 0$
$K" = 0\Delta^2 + 1\Delta + 0$
$K" = 0\Delta^2 + (1/2)\Delta + 0$
$K" = 0\Delta^2 + (1/16)\Delta + 0$
0
| Δ |
= ABS (Fast Initial Power Estimate
- Slow Initial Power Estimate)
Maximum
(Normalized to 1)
(1 * Fast Initial + 0 * Slow Initial)
Fast Initial
Power Estimate
2358
Dominates
(0.5 * Fast Initial + 0.5 * Slow Initial)
Slow Initial
Power Estimate
2367
Dominates
(0 * Fast Initial + 1 * Slow Initial)

FIG. 24E

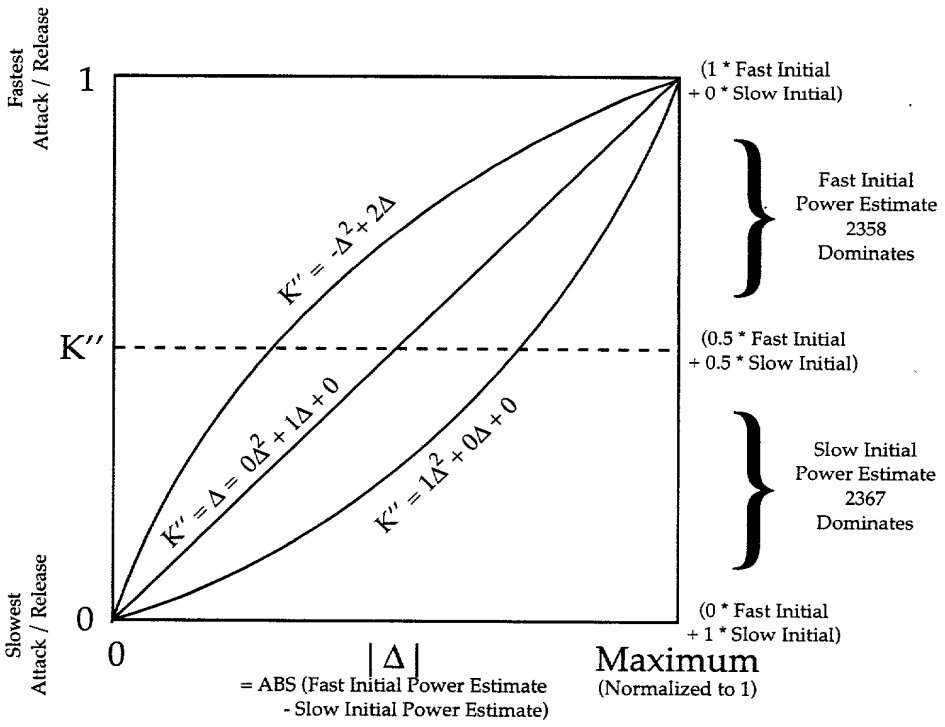

Fastest
Attack / Release
1
K''
0
Slowest
Attack / Release
(1 * Fast Initial
+ 0 * Slow Initial)
Fast Initial
Power Estimate
2358
Dominates
(0.5 * Fast Initial
+ 0.5 * Slow Initial)
Slow Initial
Power Estimate
2367
Dominates
(0 * Fast Initial
+ 1 * Slow Initial)
K'' = -Δ² + 2Δ
K'' = Δ = 0Δ² + 1Δ + 0
K'' = 1Δ² + 0Δ + 0
0
|Δ|
= ABS (Fast Initial Power Estimate
- Slow Initial Power Estimate)
Maximum
(Normalized to 1)

FIG. 24F

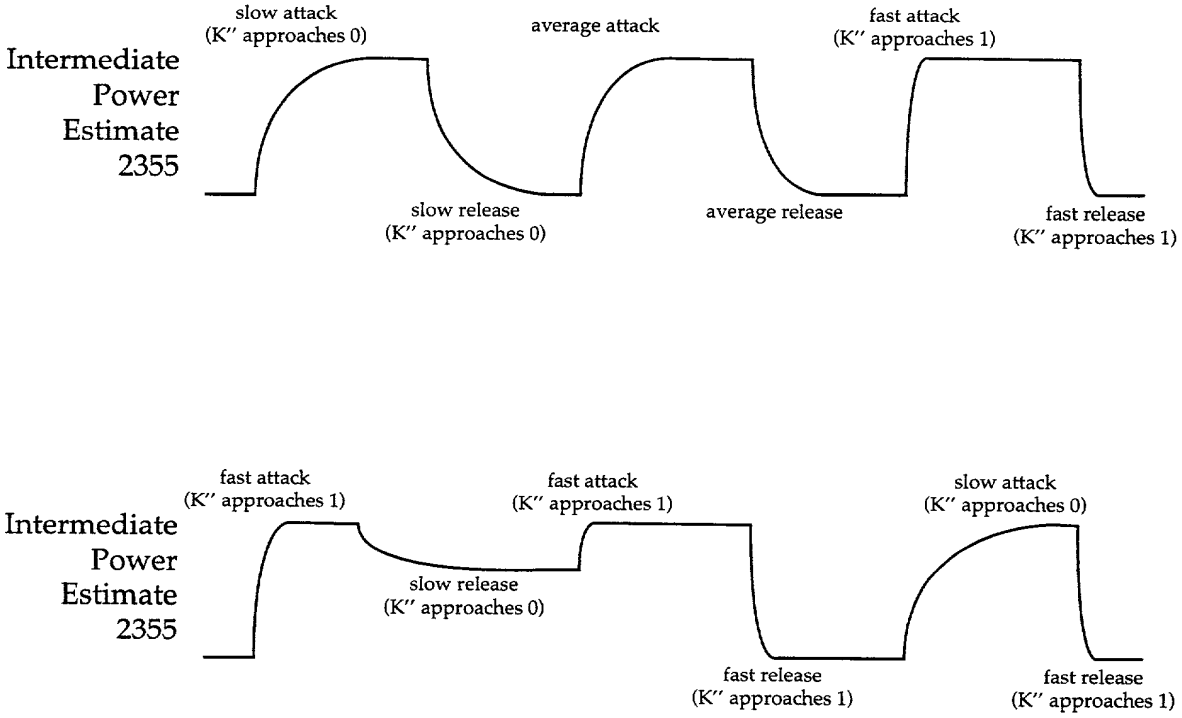

Intermediate Power Estimate 2355
slow attack (K'' approaches 0)
average attack
fast attack (K'' approaches 1)
slow release (K'' approaches 0)
average release
fast release (K'' approaches 1)
Intermediate Power Estimate 2355
fast attack (K'' approaches 1)
fast attack (K'' approaches 1)
slow attack (K'' approaches 0)
slow release (K'' approaches 0)
fast release (K'' approaches 1)
fast release (K'' approaches 1)

FIG. 24G

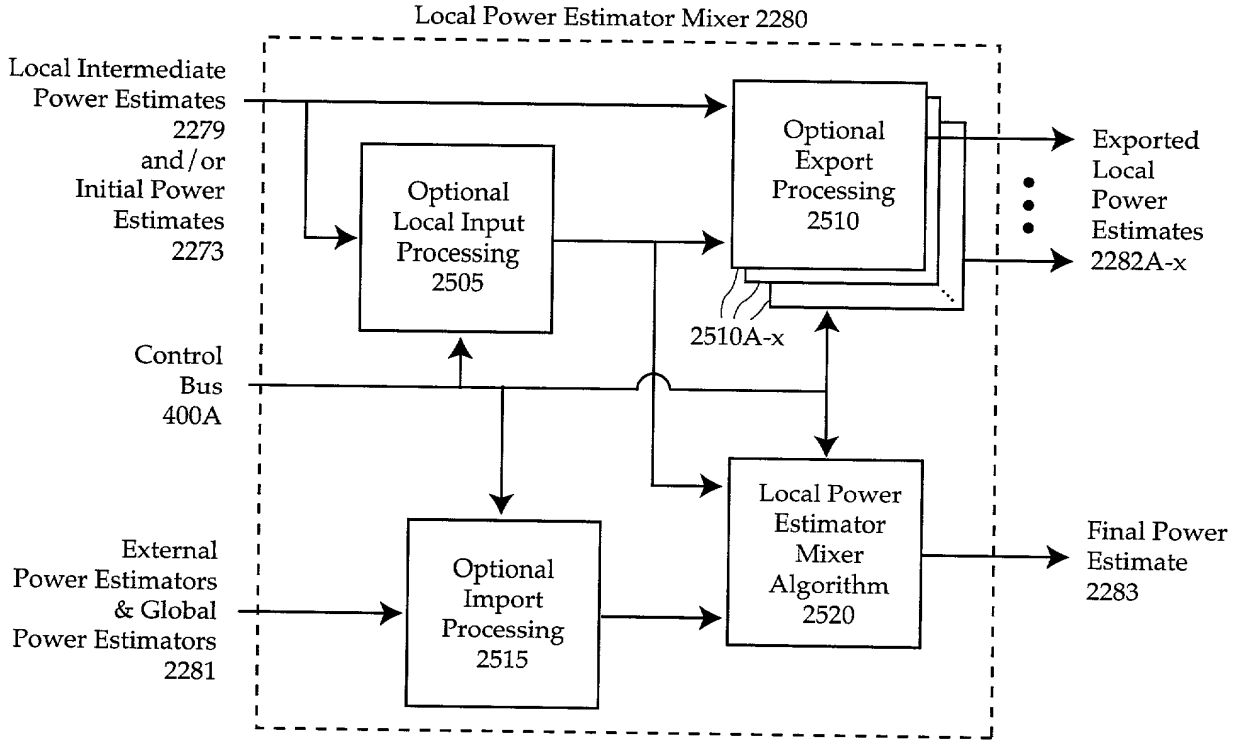


FIG. 25A

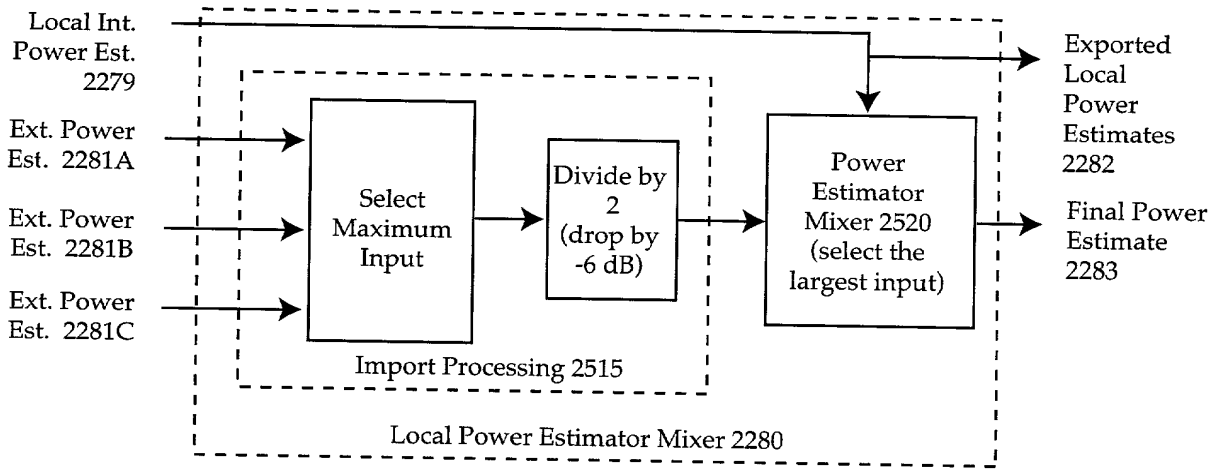


FIG. 25B

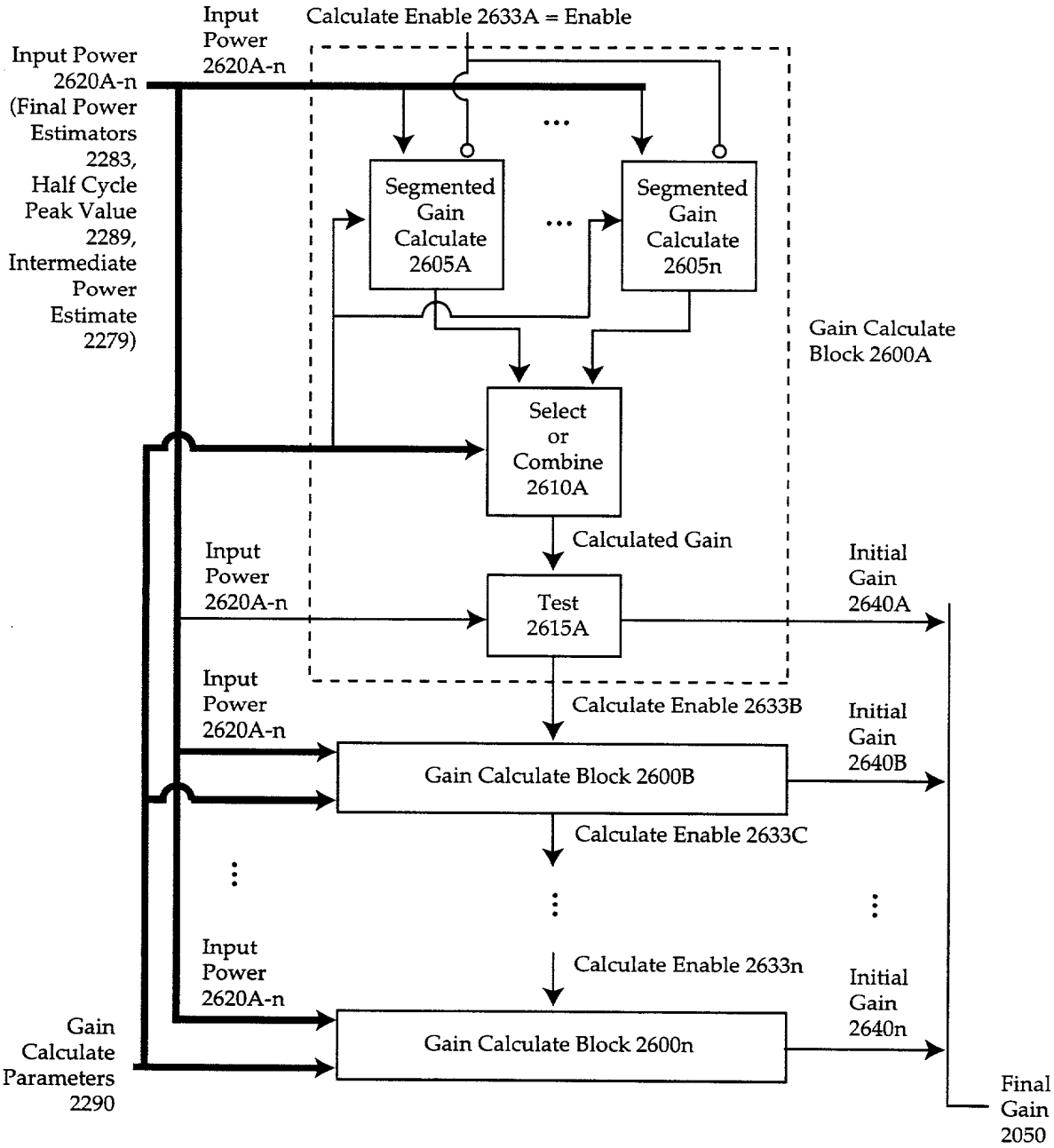

Input Power 2620A-n (Final Power Estimators 2283, Half Cycle Peak Value 2289, Intermediate Power Estimate 2279)
Input Power 2620A-n
Calculate Enable 2633A = Enable
Segmented Gain Calculate 2605A
Segmented Gain Calculate 2605n
Gain Calculate Block 2600A
Select or Combine 2610A
Calculated Gain
Input Power 2620A-n
Test 2615A
Initial Gain 2640A
Input Power 2620A-n
Calculate Enable 2633B
Gain Calculate Block 2600B
Initial Gain 2640B
Calculate Enable 2633C
Input Power 2620A-n
Calculate Enable 2633n
Gain Calculate Block 2600n
Initial Gain 2640n
Gain Calculate Parameters 2290
Final Gain 2050

FIG. 26A

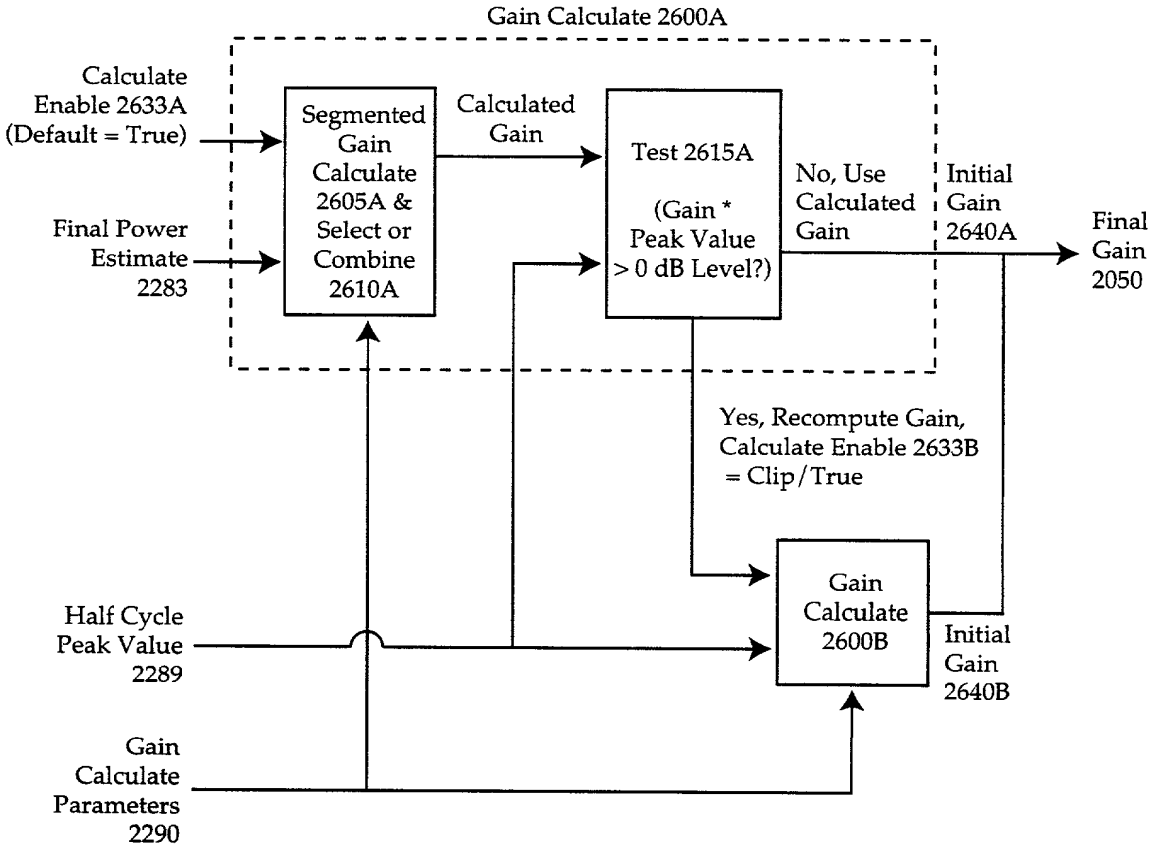

Gain Calculate 2600A
Calculate Enable 2633A (Default = True)
Final Power Estimate 2283
Segmented Gain Calculate 2605A & Select or Combine 2610A
Calculated Gain
Test 2615A
(Gain * Peak Value > 0 dB Level?)
No, Use Calculated Gain
Initial Gain 2640A
Final Gain 2050
Yes, Recompute Gain, Calculate Enable 2633B = Clip/True
Gain Calculate 2600B
Initial Gain 2640B
Half Cycle Peak Value 2289
Gain Calculate Parameters 2290

FIG. 26B

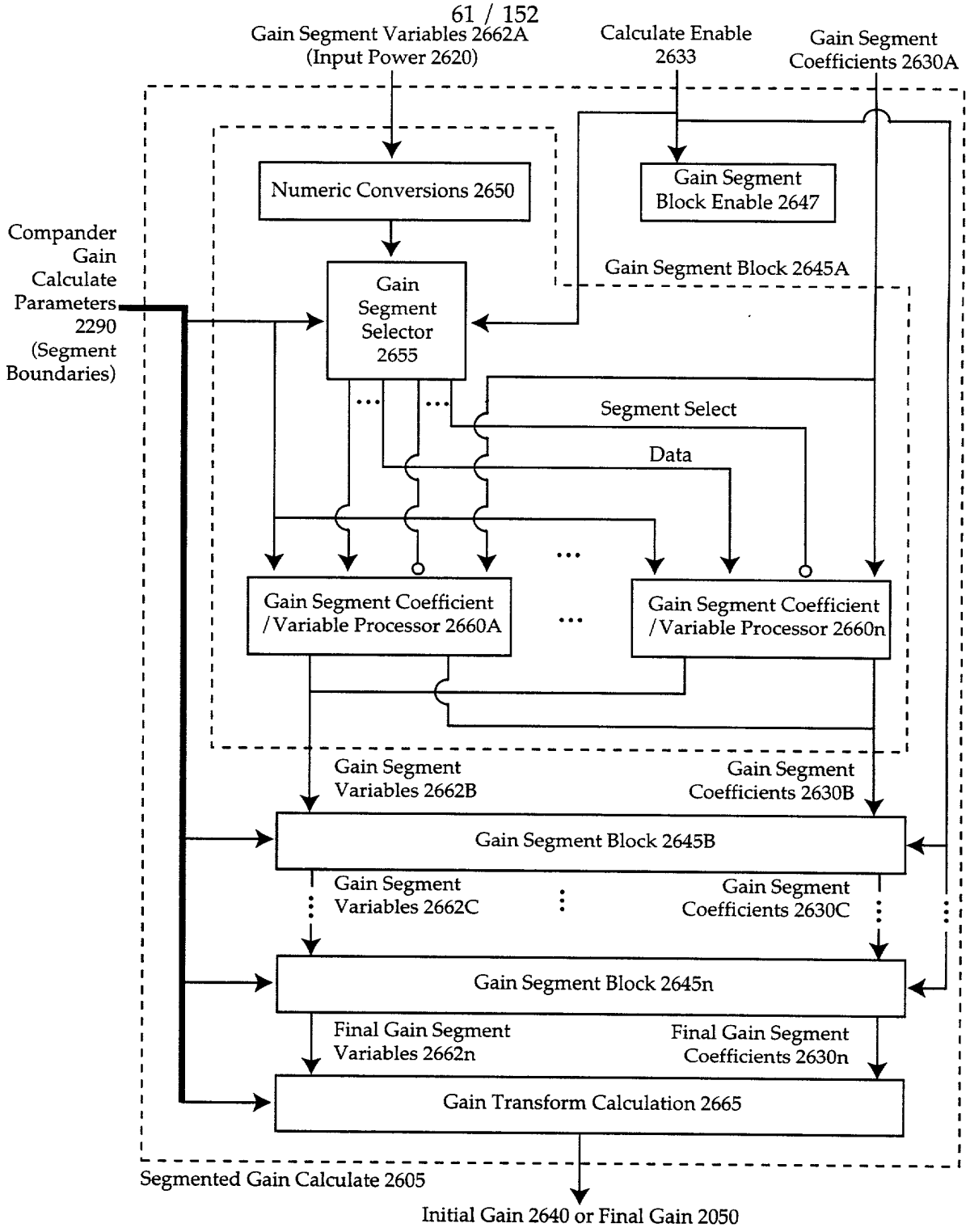

Gain Segment Variables 2662A
(Input Power 2620)
Calculate Enable
2633
Gain Segment
Coefficients 2630A
Numeric Conversions 2650
Gain Segment
Block Enable 2647
Compander
Gain
Calculate
Parameters
2290
(Segment
Boundaries)
Gain Segment Block 2645A
Gain
Segment
Selector
2655
Segment Select
Data
Gain Segment Coefficient
/Variable Processor 2660A
Gain Segment Coefficient
/Variable Processor 2660n
Gain Segment
Variables 2662B
Gain Segment
Coefficients 2630B
Gain Segment Block 2645B
Gain Segment
Variables 2662C
Gain Segment
Coefficients 2630C
Gain Segment Block 2645n
Final Gain Segment
Variables 2662n
Final Gain Segment
Coefficients 2630n
Gain Transform Calculation 2665
Segmented Gain Calculate 2605
Initial Gain 2640 or Final Gain 2050

FIG. 26C

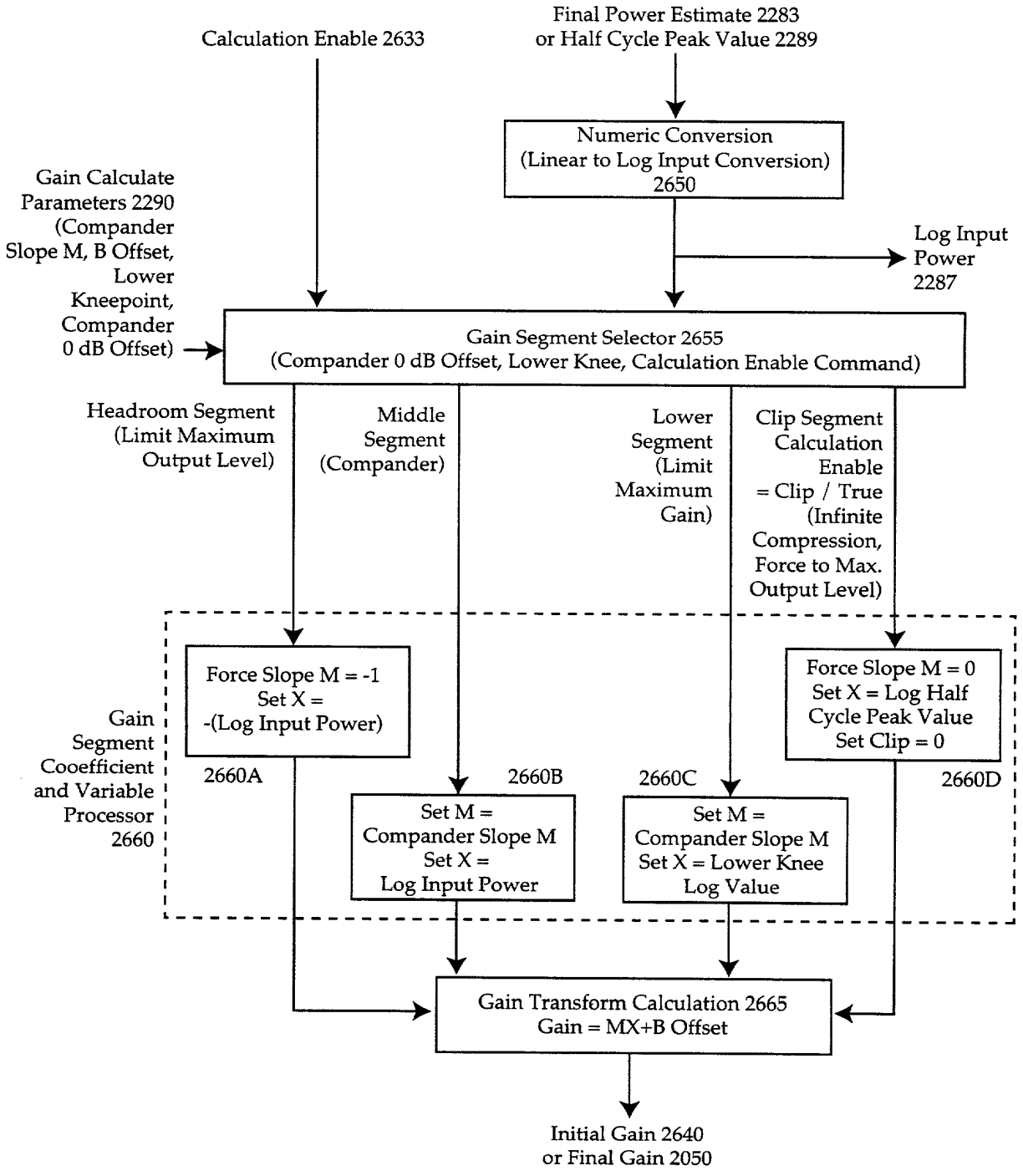

Calculation Enable 2633
Final Power Estimate 2283
or Half Cycle Peak Value 2289
Numeric Conversion
(Linear to Log Input Conversion)
2650
Gain Calculate
Parameters 2290
(Compander
Slope M, B Offset,
Lower
Kneepoint,
Compander
0 dB Offset)
Log Input
Power
2287
Gain Segment Selector 2655
(Compander 0 dB Offset, Lower Knee, Calculation Enable Command)
Headroom Segment
(Limit Maximum
Output Level)
Middle
Segment
(Compander)
Lower
Segment
(Limit
Maximum
Gain)
Clip Segment
Calculation
Enable
= Clip / True
(Infinite
Compression,
Force to Max.
Output Level)
Gain
Segment
Cooefficient
and Variable
Processor
2660
Force Slope M = -1
Set X =
-(Log Input Power)
2660A
Set M =
Compander Slope M
Set X =
Log Input Power
2660B
Set M =
Compander Slope M
Set X = Lower Knee
Log Value
2660C
Force Slope M = 0
Set X = Log Half
Cycle Peak Value
Set Clip = 0
2660D
Gain Transform Calculation 2665
Gain = MX+B Offset
Initial Gain 2640
or Final Gain 2050

FIG. 26D

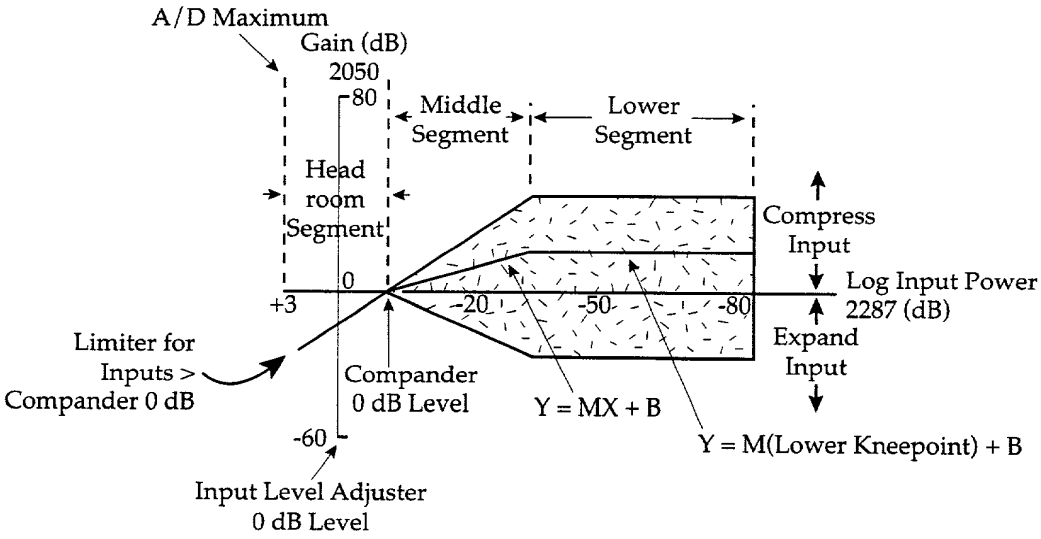


FIG. 26E

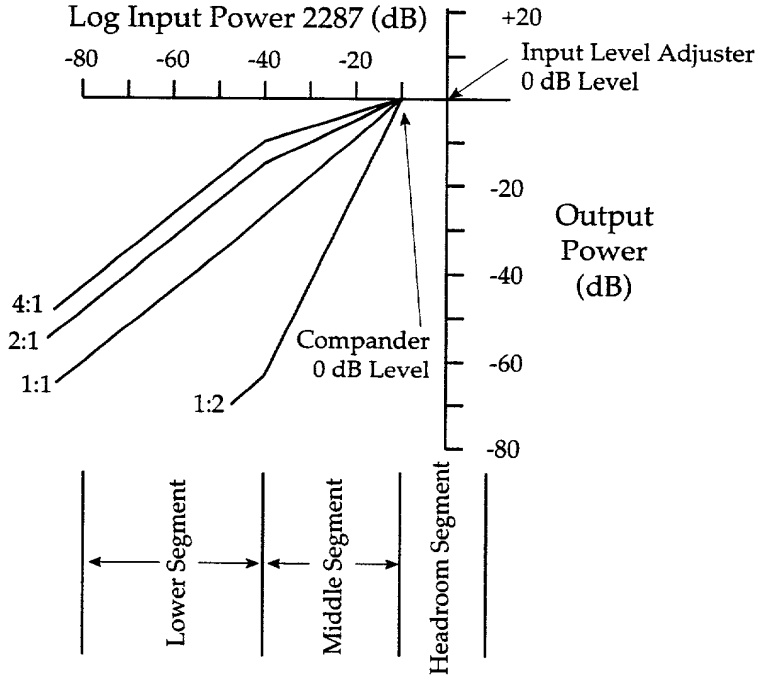


FIG. 26F

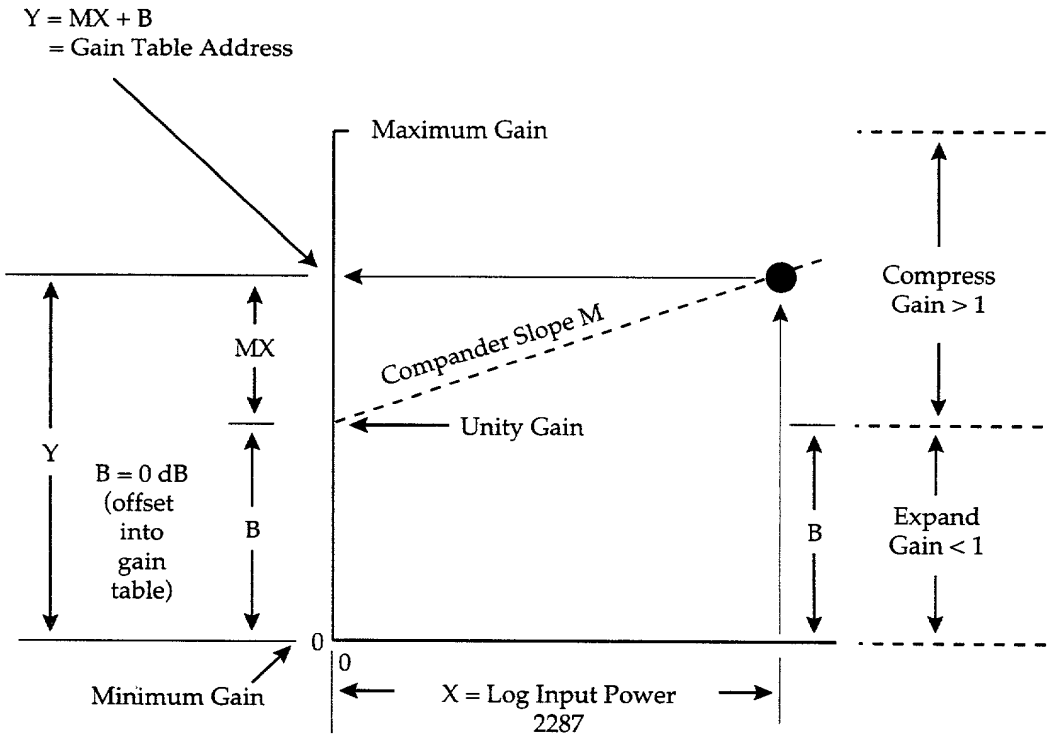

Y = MX + B
= Gain Table Address
Maximum Gain
Compress
Gain > 1
MX
Compander Slope M
Unity Gain
Y
B = 0 dB
(offset
into
gain
table)
B
B
Expand
Gain < 1
0
0
Minimum Gain
X = Log Input Power
2287

FIG. 26G

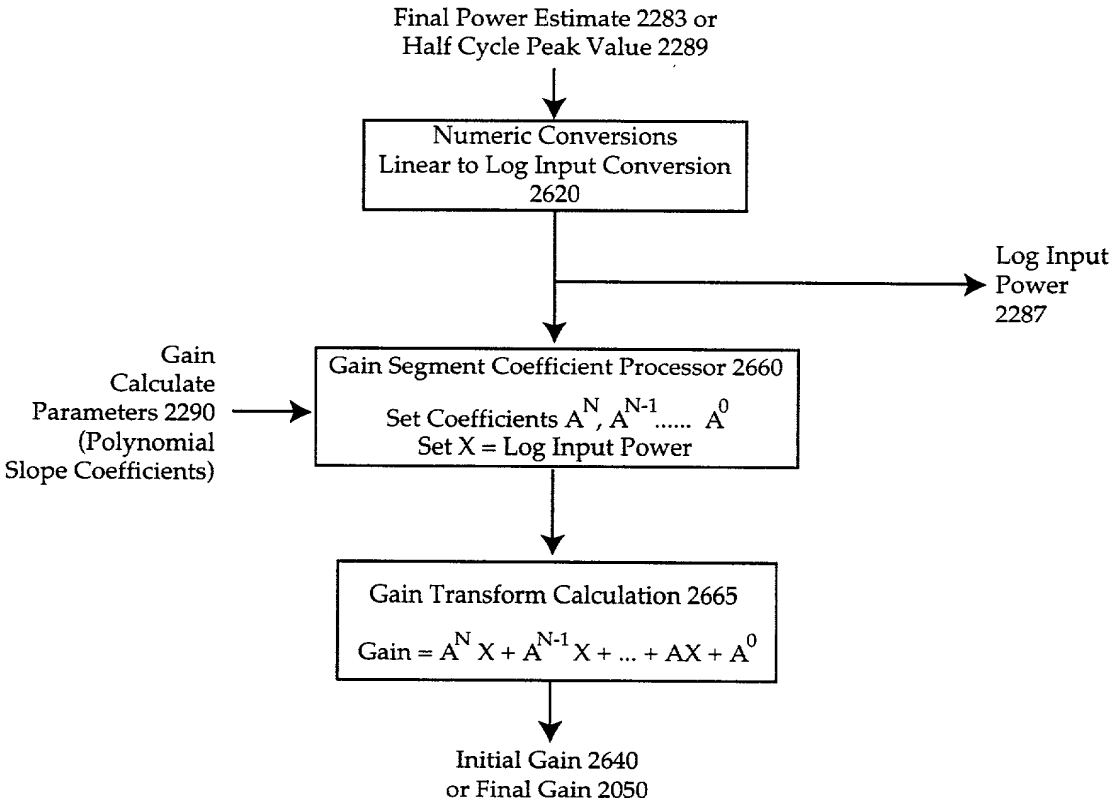

Final Power Estimate 2283 or
Half Cycle Peak Value 2289
Numeric Conversions
Linear to Log Input Conversion
2620
Log Input
Power
2287
Gain
Calculate
Parameters 2290
(Polynomial
Slope Coefficients)
Gain Segment Coefficient Processor 2660
Set Coefficients A^N, A^{N-1}..... A^0
Set X = Log Input Power
Gain Transform Calculation 2665
Gain = $A^N X + A^{N-1} X + ... + AX + A^0$
Initial Gain 2640
or Final Gain 2050

FIG. 26H

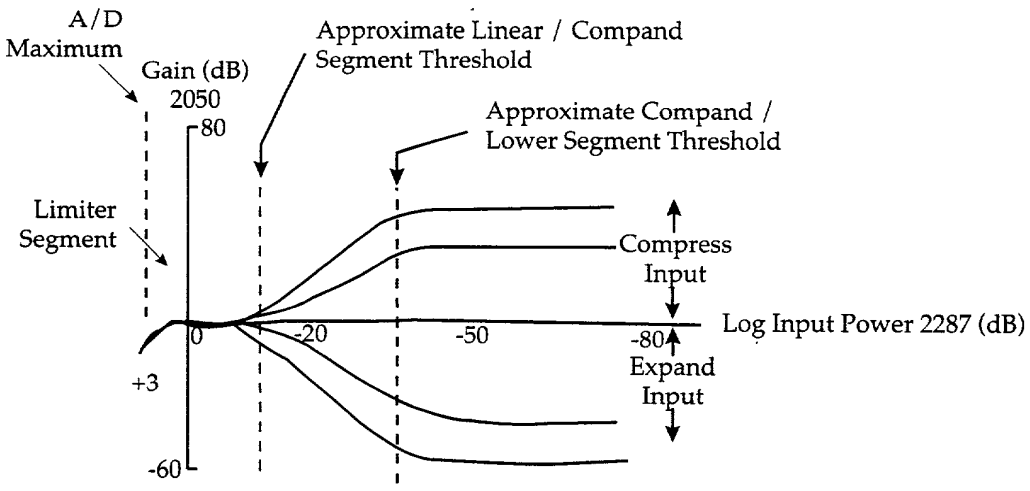


FIG. 26I

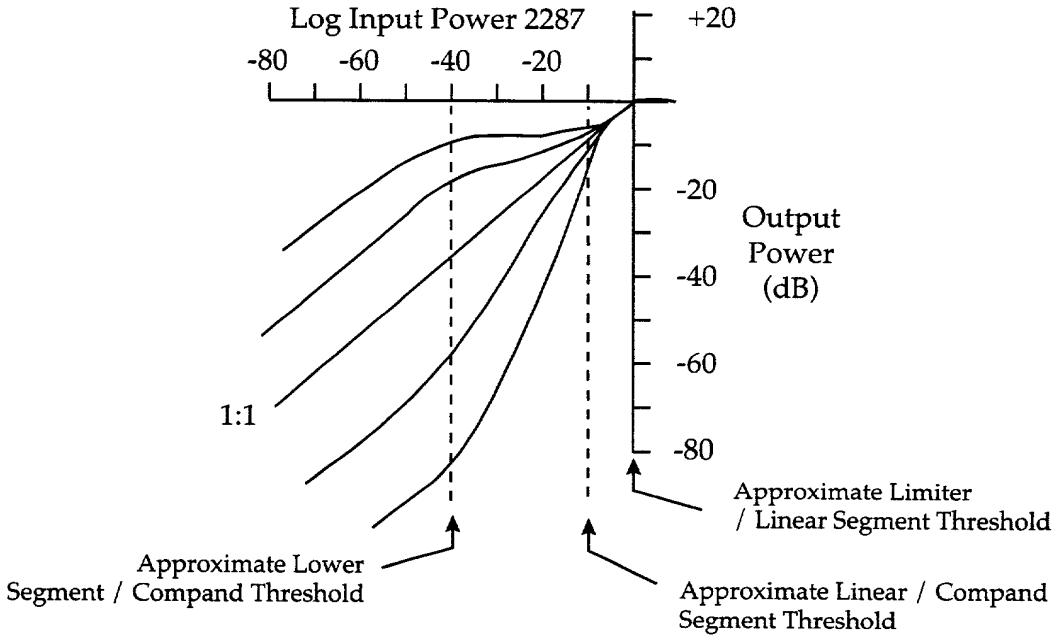


FIG. 26J

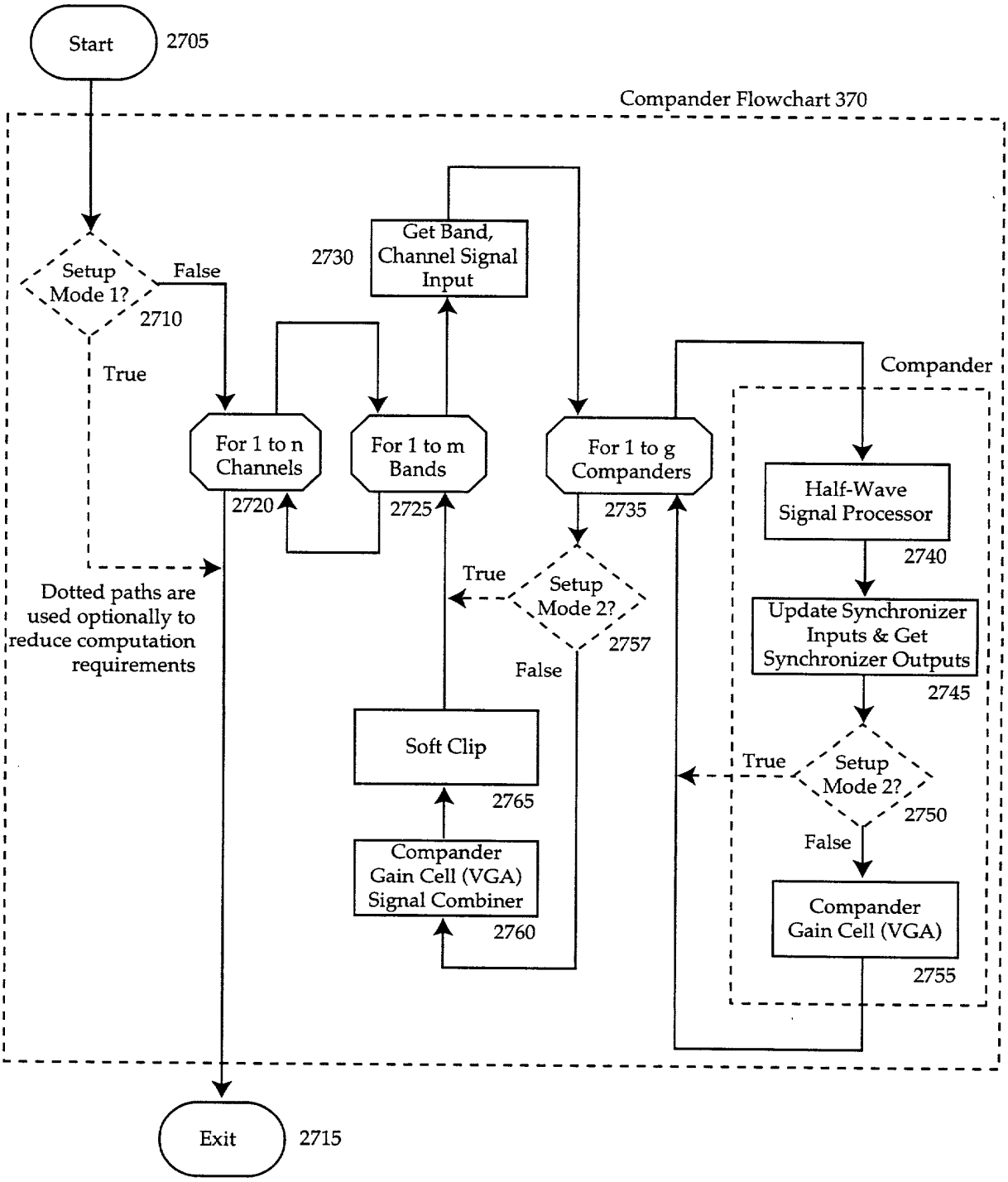

Start
2705
Compander Flowchart 370
Setup Mode 1?
2710
False
True
Get Band, Channel Signal Input
2730
For 1 to n Channels
2720
For 1 to m Bands
2725
For 1 to g Companders
2735
Compander
Half-Wave Signal Processor
2740
Update Synchronizer Inputs & Get Synchronizer Outputs
2745
Setup Mode 2?
2750
True
False
Compander Gain Cell (VGA)
2755
Setup Mode 2?
2757
True
False
Soft Clip
2765
Compander Gain Cell (VGA) Signal Combiner
2760
Dotted paths are used optionally to reduce computation requirements
Exit
2715

FIG. 27A

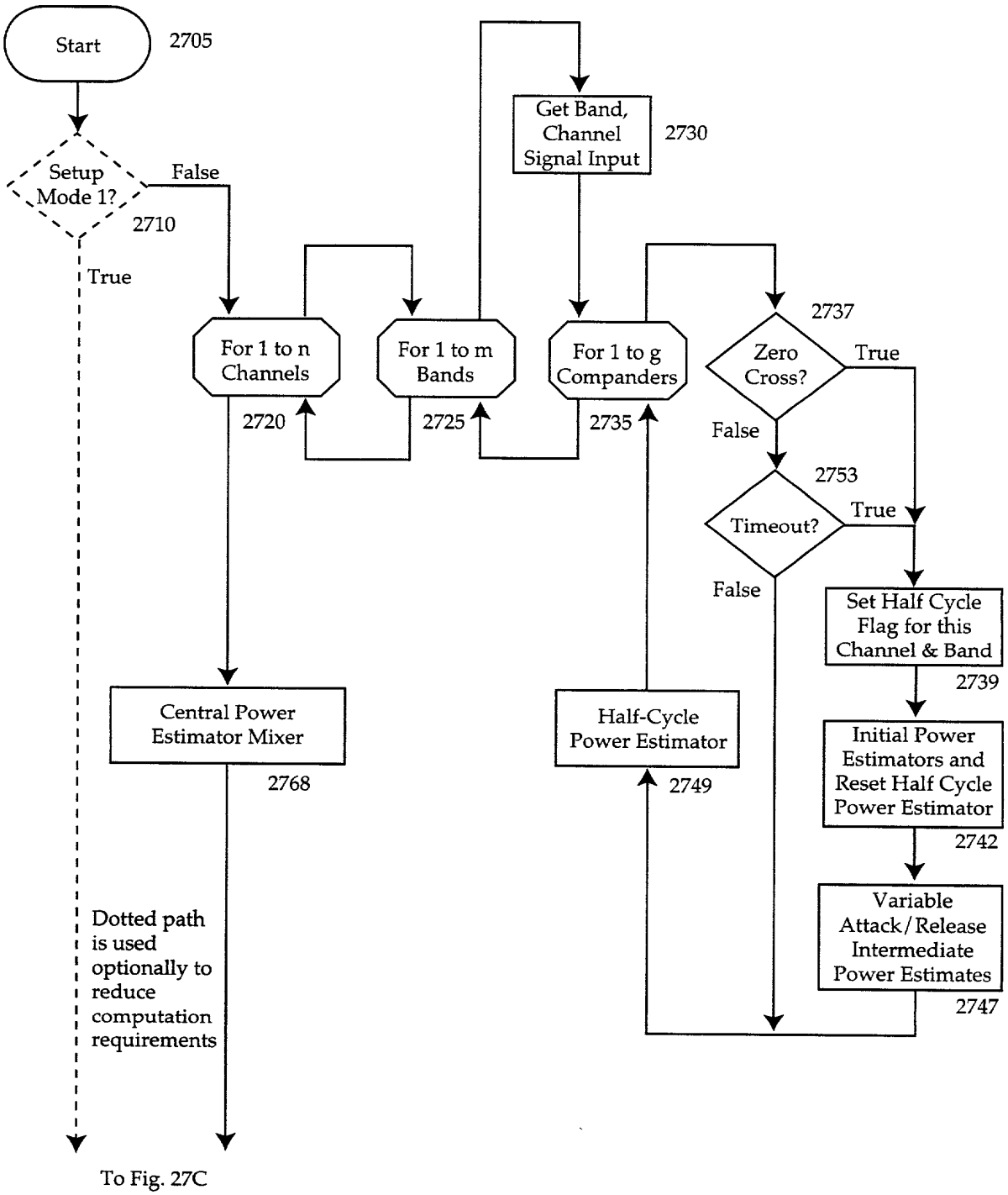

Start
2705
Setup Mode 1?
2710
False
True
Get Band, Channel Signal Input
2730
For 1 to n Channels
2720
For 1 to m Bands
2725
For 1 to g Companders
2735
2737
Zero Cross?
True
False
2753
Timeout?
True
False
Set Half Cycle Flag for this Channel & Band
2739
Initial Power Estimators and Reset Half Cycle Power Estimator
2742
Variable Attack/Release Intermediate Power Estimates
2747
Central Power Estimator Mixer
2768
Half-Cycle Power Estimator
2749
Dotted path is used optionally to reduce computation requirements
To Fig. 27C

FIG. 27B

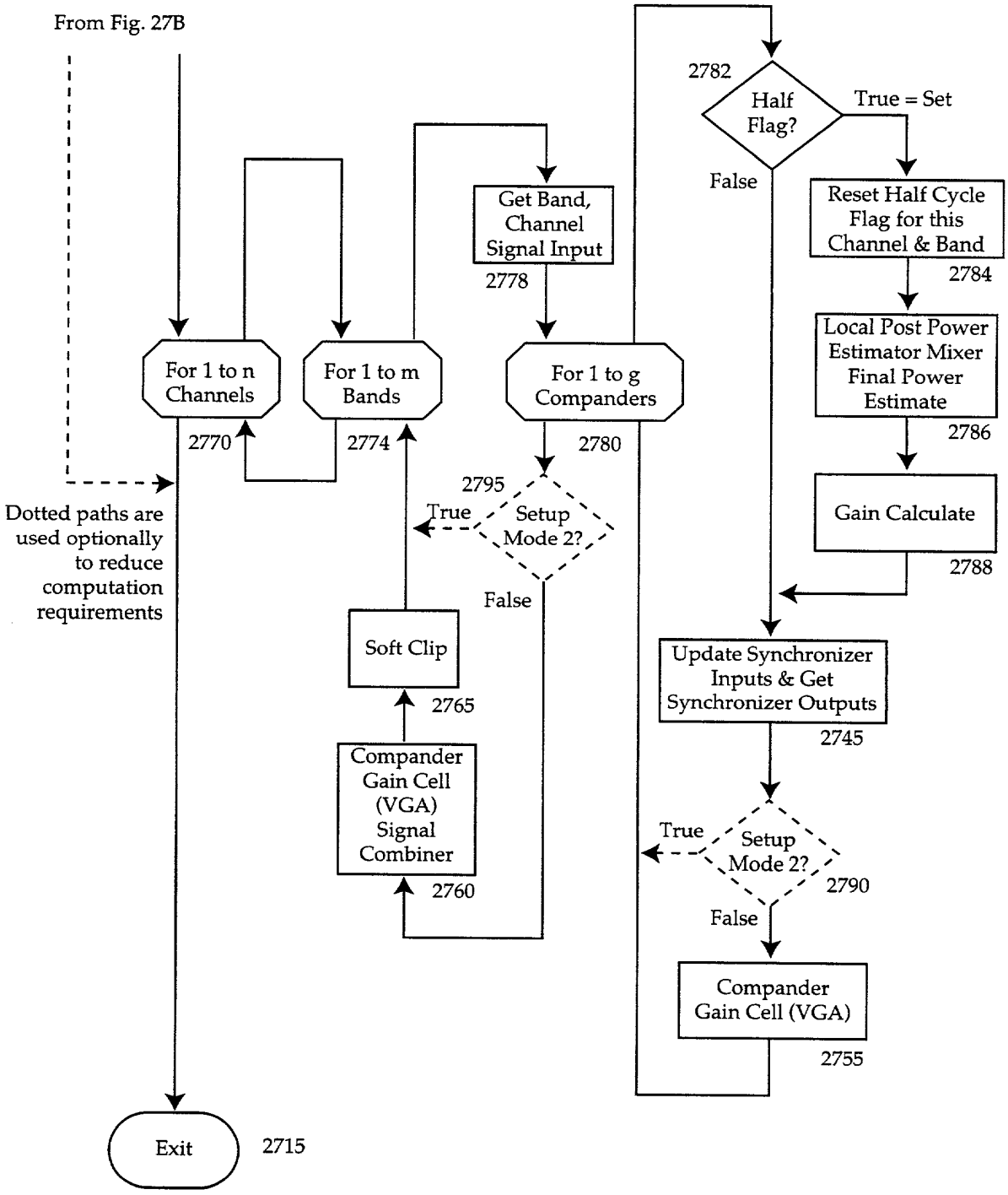

From Fig. 27B
Dotted paths are used optionally to reduce computation requirements
For 1 to n Channels
2770
For 1 to m Bands
2774
Get Band, Channel Signal Input
2778
For 1 to g Companders
2780
2795
True
Setup Mode 2?
False
Soft Clip
2765
Compander Gain Cell (VGA) Signal Combiner
2760
2782
Half Flag?
True = Set
False
Reset Half Cycle Flag for this Channel & Band
2784
Local Post Power Estimator Mixer Final Power Estimate
2786
Gain Calculate
2788
Update Synchronizer Inputs & Get Synchronizer Outputs
2745
True
Setup Mode 2?
2790
False
Compander Gain Cell (VGA)
2755
Exit
2715

FIG. 27C

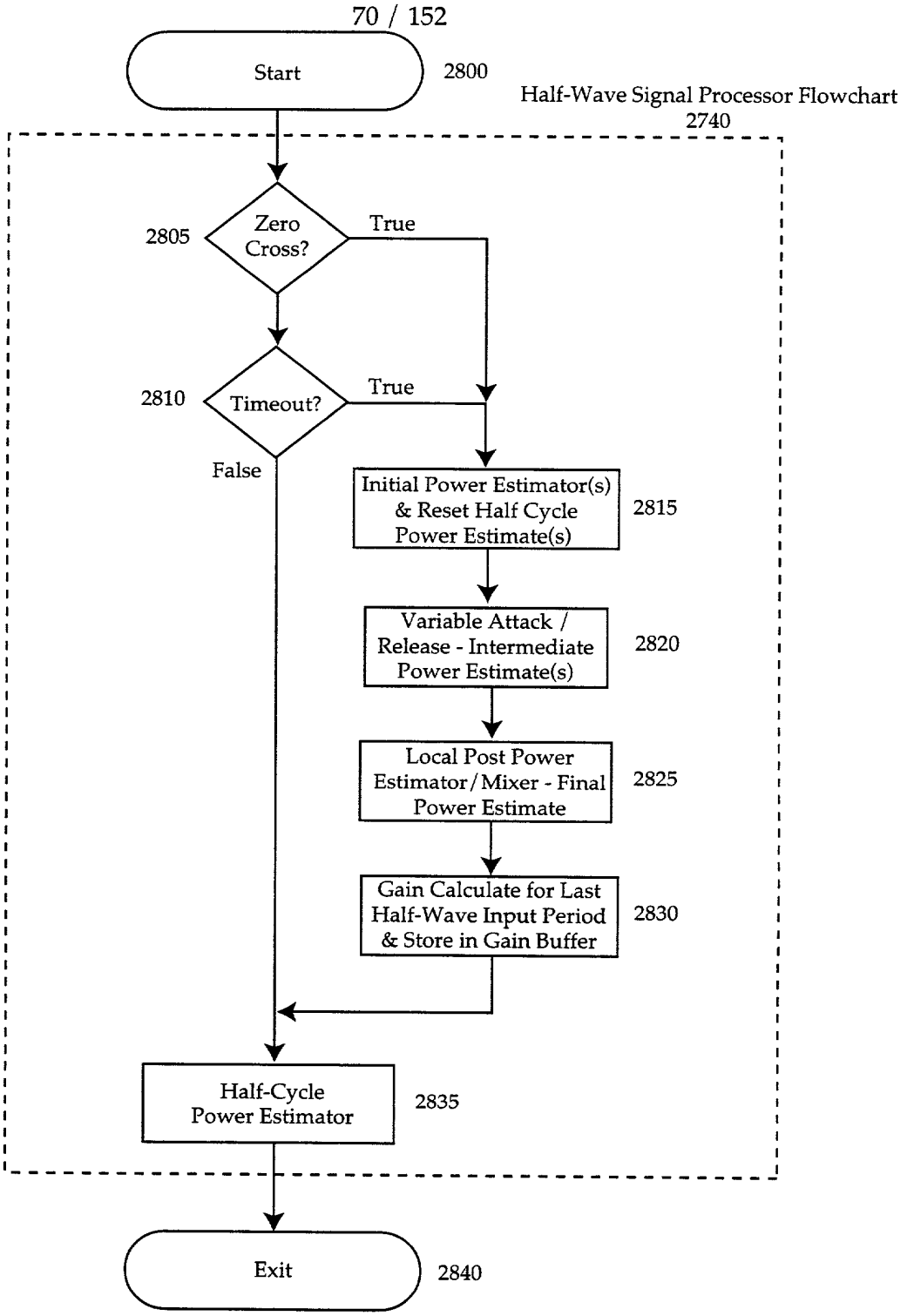

Start
2800
Half-Wave Signal Processor Flowchart
2740
2805
Zero Cross?
True
2810
Timeout?
True
False
Initial Power Estimator(s) & Reset Half Cycle Power Estimate(s)
2815
Variable Attack / Release - Intermediate Power Estimate(s)
2820
Local Post Power Estimator / Mixer - Final Power Estimate
2825
Gain Calculate for Last Half-Wave Input Period & Store in Gain Buffer
2830
Half-Cycle Power Estimator
2835
Exit
2840

FIG. 28

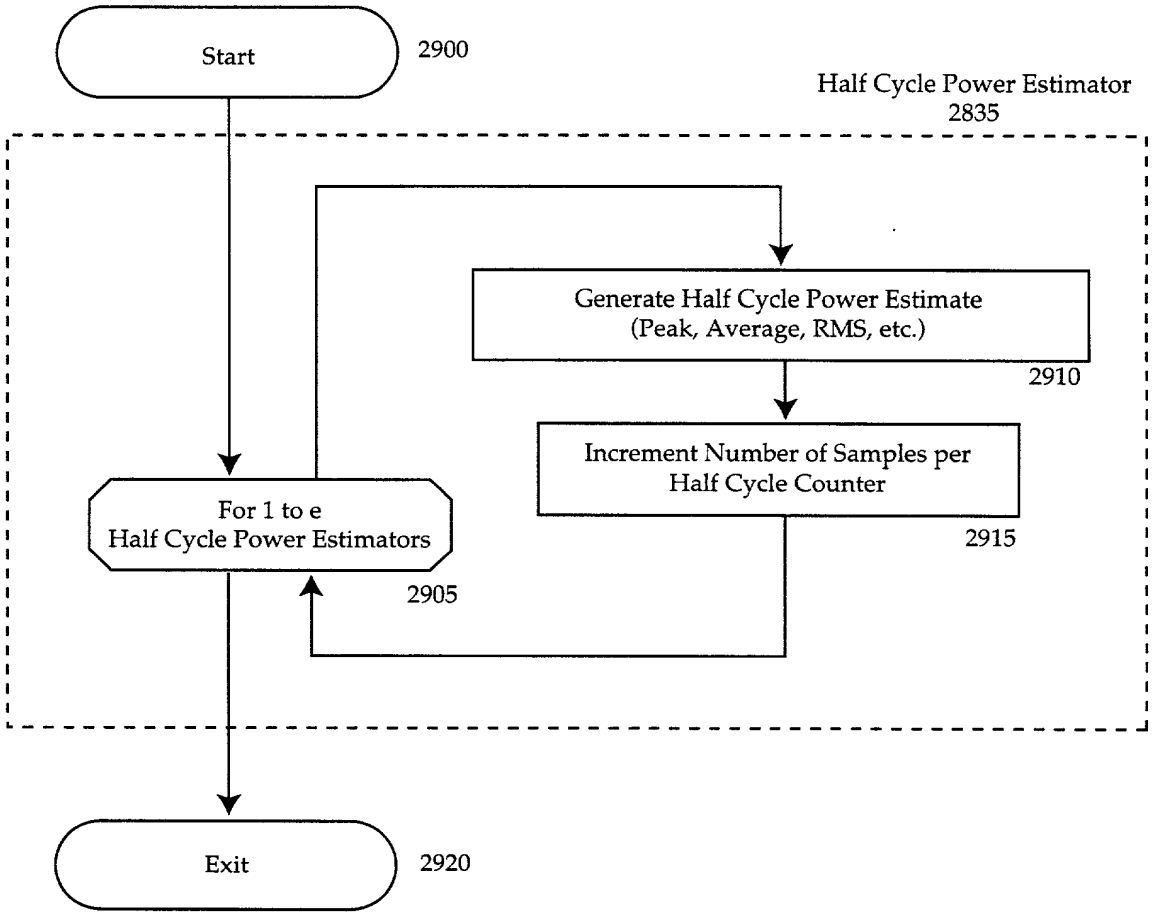

Start
2900
Half Cycle Power Estimator
2835
Generate Half Cycle Power Estimate
(Peak, Average, RMS, etc.)
2910
Increment Number of Samples per
Half Cycle Counter
2915
For 1 to e
Half Cycle Power Estimators
2905
Exit
2920

FIG. 29

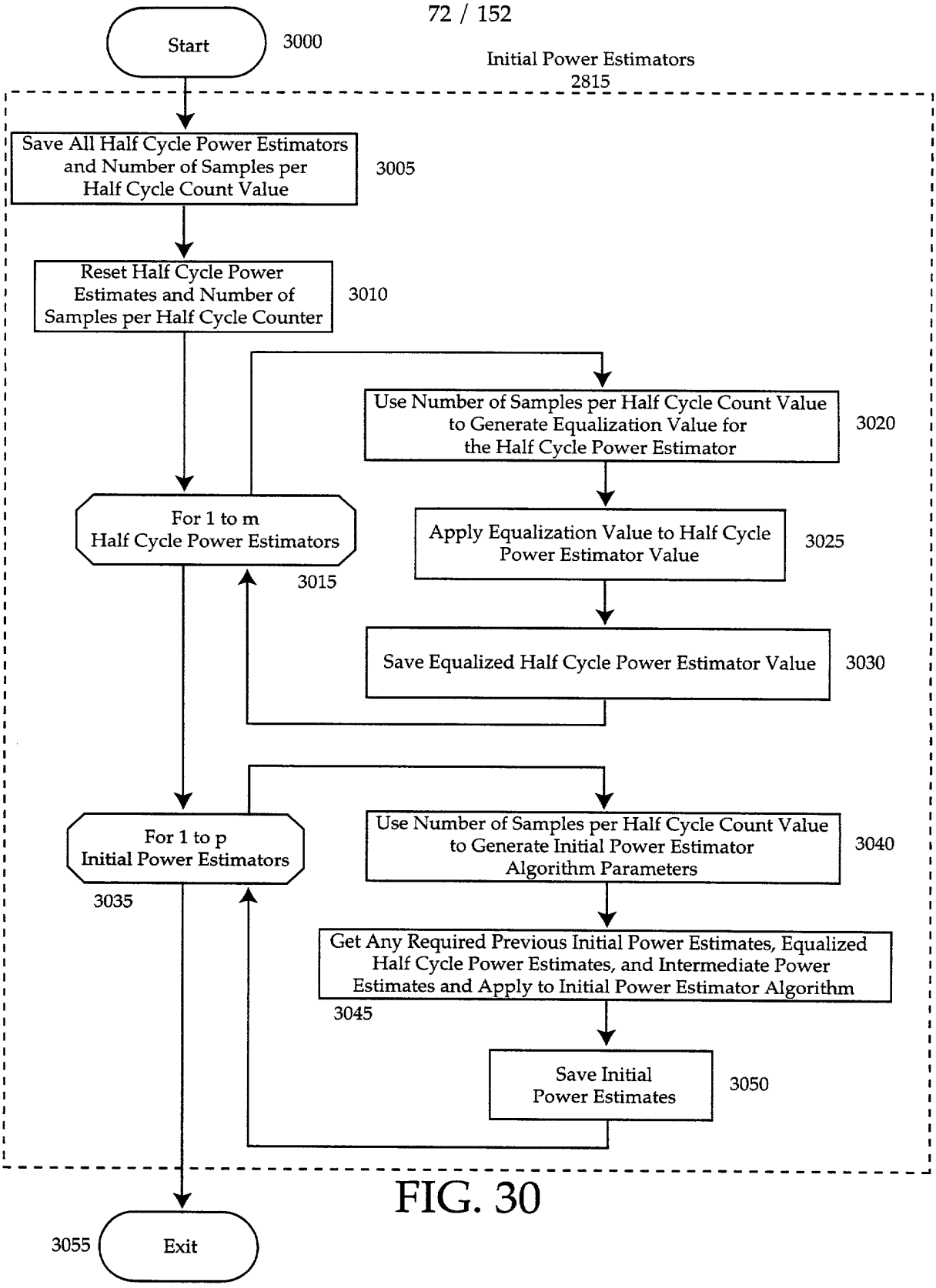

Start
3000
Initial Power Estimators
2815
Save All Half Cycle Power Estimators and Number of Samples per Half Cycle Count Value
3005
Reset Half Cycle Power Estimates and Number of Samples per Half Cycle Counter
3010
Use Number of Samples per Half Cycle Count Value to Generate Equalization Value for the Half Cycle Power Estimator
3020
For 1 to m Half Cycle Power Estimators
3015
Apply Equalization Value to Half Cycle Power Estimator Value
3025
Save Equalized Half Cycle Power Estimator Value
3030
For 1 to p Initial Power Estimators
3035
Use Number of Samples per Half Cycle Count Value to Generate Initial Power Estimator Algorithm Parameters
3040
Get Any Required Previous Initial Power Estimates, Equalized Half Cycle Power Estimates, and Intermediate Power Estimates and Apply to Initial Power Estimator Algorithm
3045
Save Initial Power Estimates
3050
3055
Exit

FIG. 30

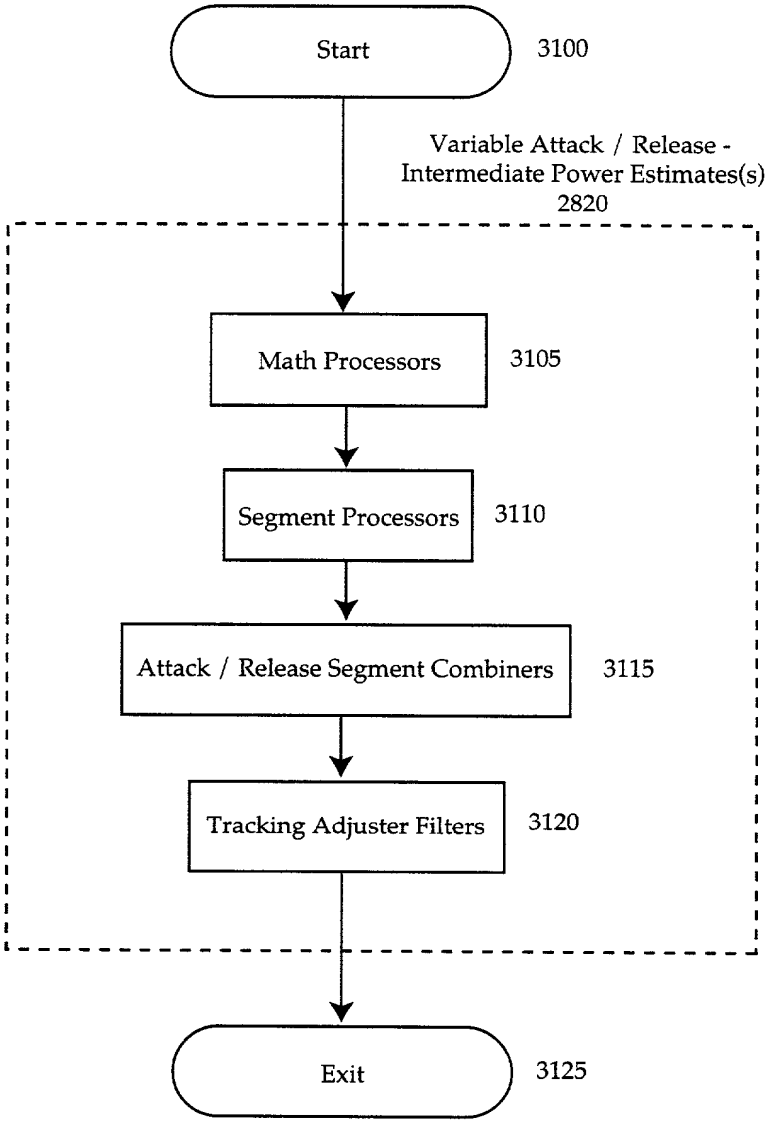

Start
3100
Variable Attack / Release -
Intermediate Power Estimates(s)
2820
Math Processors
3105
Segment Processors
3110
Attack / Release Segment Combiners
3115
Tracking Adjuster Filters
3120
Exit
3125

FIG. 31

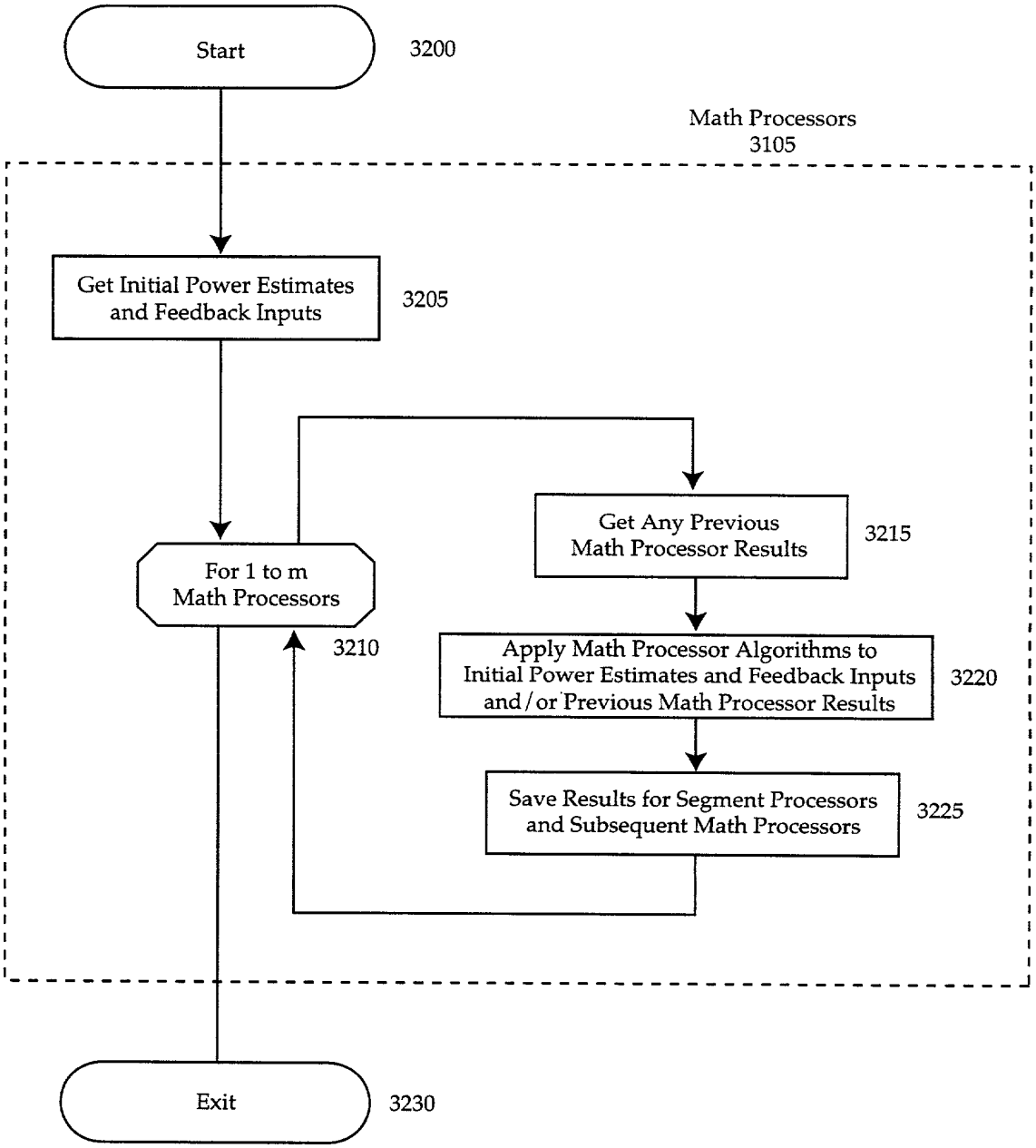

Start
3200
Math Processors
3105
Get Initial Power Estimates
and Feedback Inputs
3205
For 1 to m
Math Processors
3210
Get Any Previous
Math Processor Results
3215
Apply Math Processor Algorithms to
Initial Power Estimates and Feedback Inputs
and/or Previous Math Processor Results
3220
Save Results for Segment Processors
and Subsequent Math Processors
3225
Exit
3230

FIG. 32

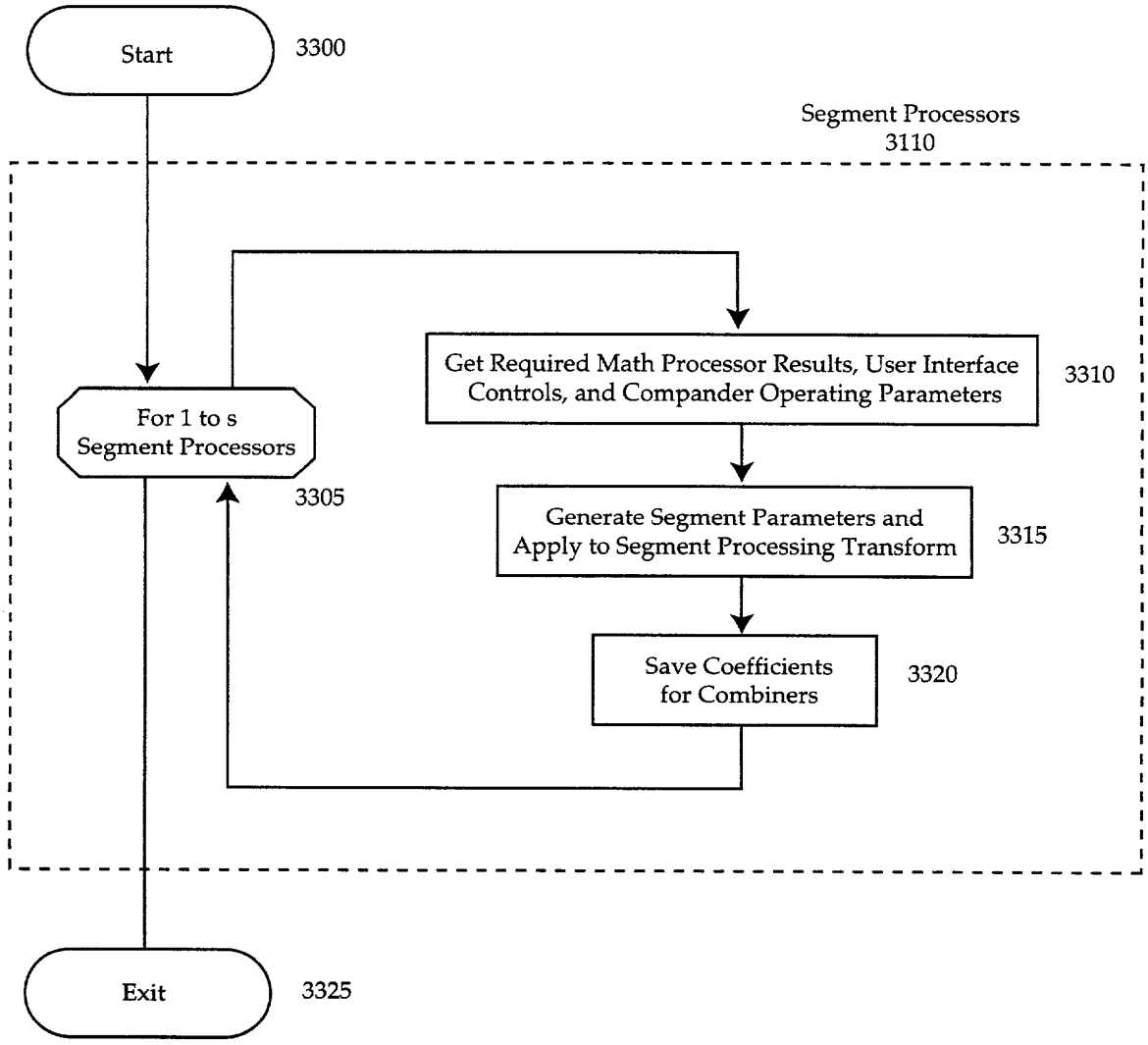

Start
3300
Segment Processors
3110
Get Required Math Processor Results, User Interface Controls, and Compander Operating Parameters
3310
For 1 to s Segment Processors
3305
Generate Segment Parameters and Apply to Segment Processing Transform
3315
Save Coefficients for Combiners
3320
Exit
3325

FIG. 33

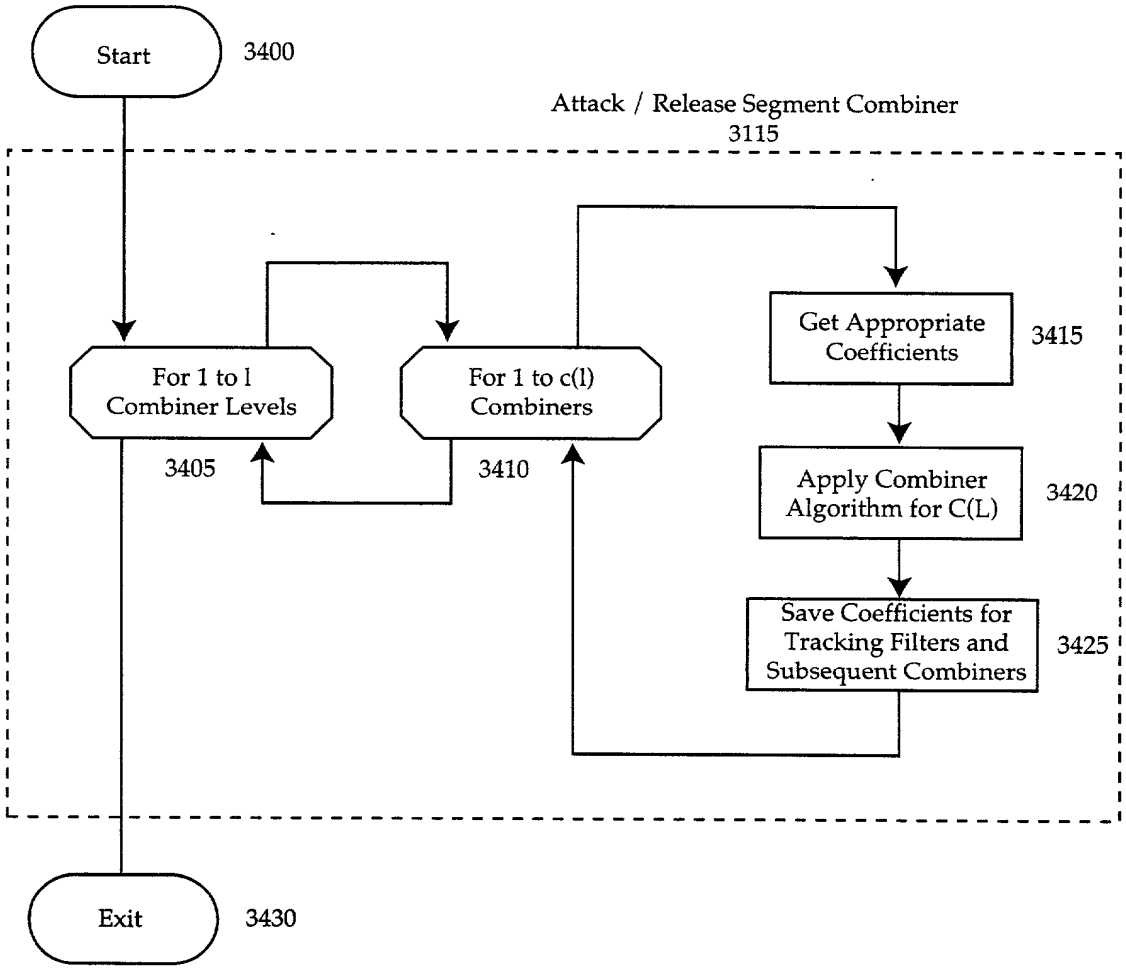

Start
3400
Attack / Release Segment Combiner
3115
For 1 to l
Combiner Levels
3405
For 1 to c(l)
Combiners
3410
Get Appropriate
Coefficients
3415
Apply Combiner
Algorithm for C(L)
3420
Save Coefficients for
Tracking Filters and
Subsequent Combiners
3425
Exit
3430

FIG. 34

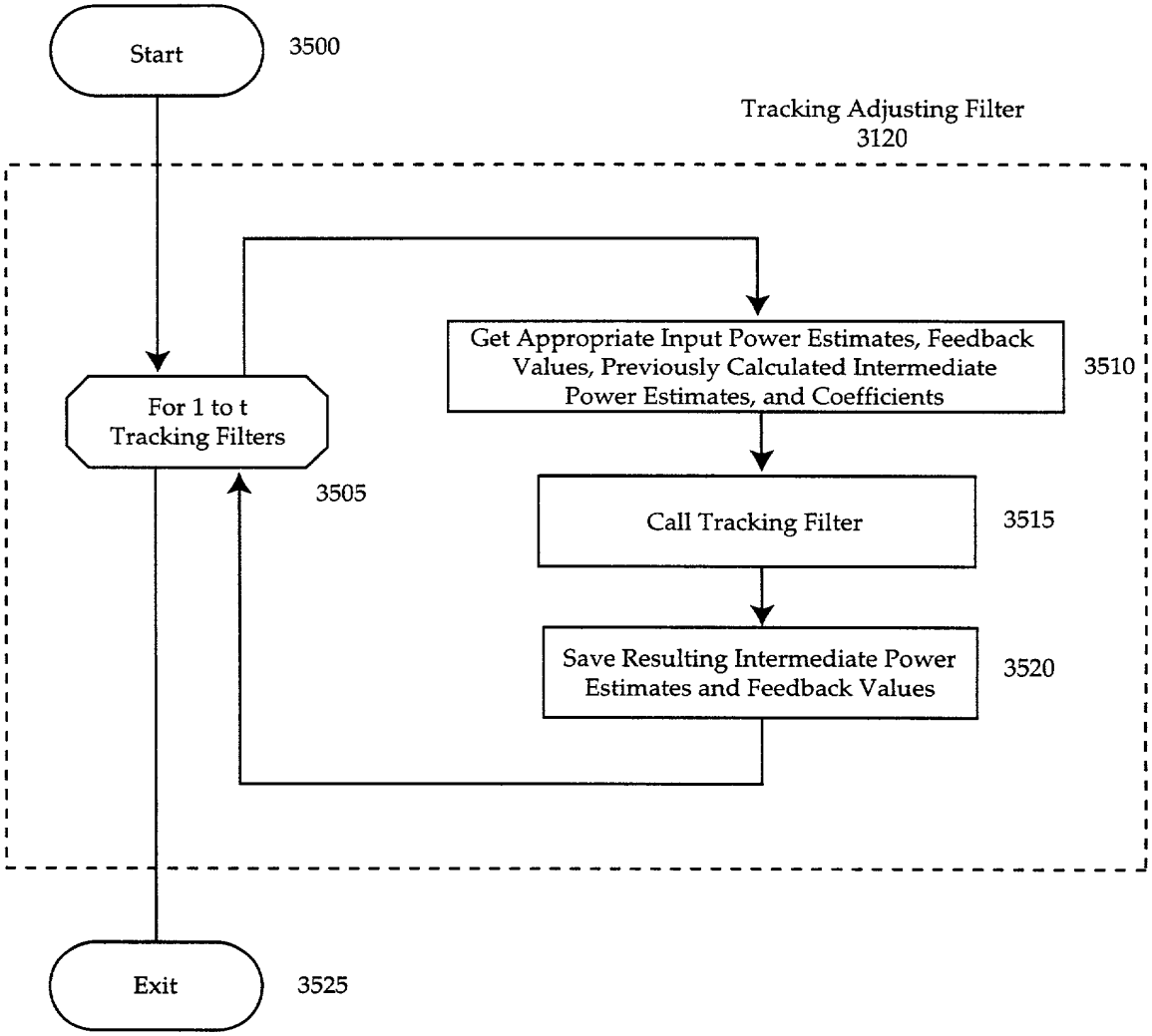

Start
3500
Tracking Adjusting Filter
3120
Get Appropriate Input Power Estimates, Feedback Values, Previously Calculated Intermediate Power Estimates, and Coefficients
3510
For 1 to t Tracking Filters
3505
Call Tracking Filter
3515
Save Resulting Intermediate Power Estimates and Feedback Values
3520
Exit
3525

FIG. 35

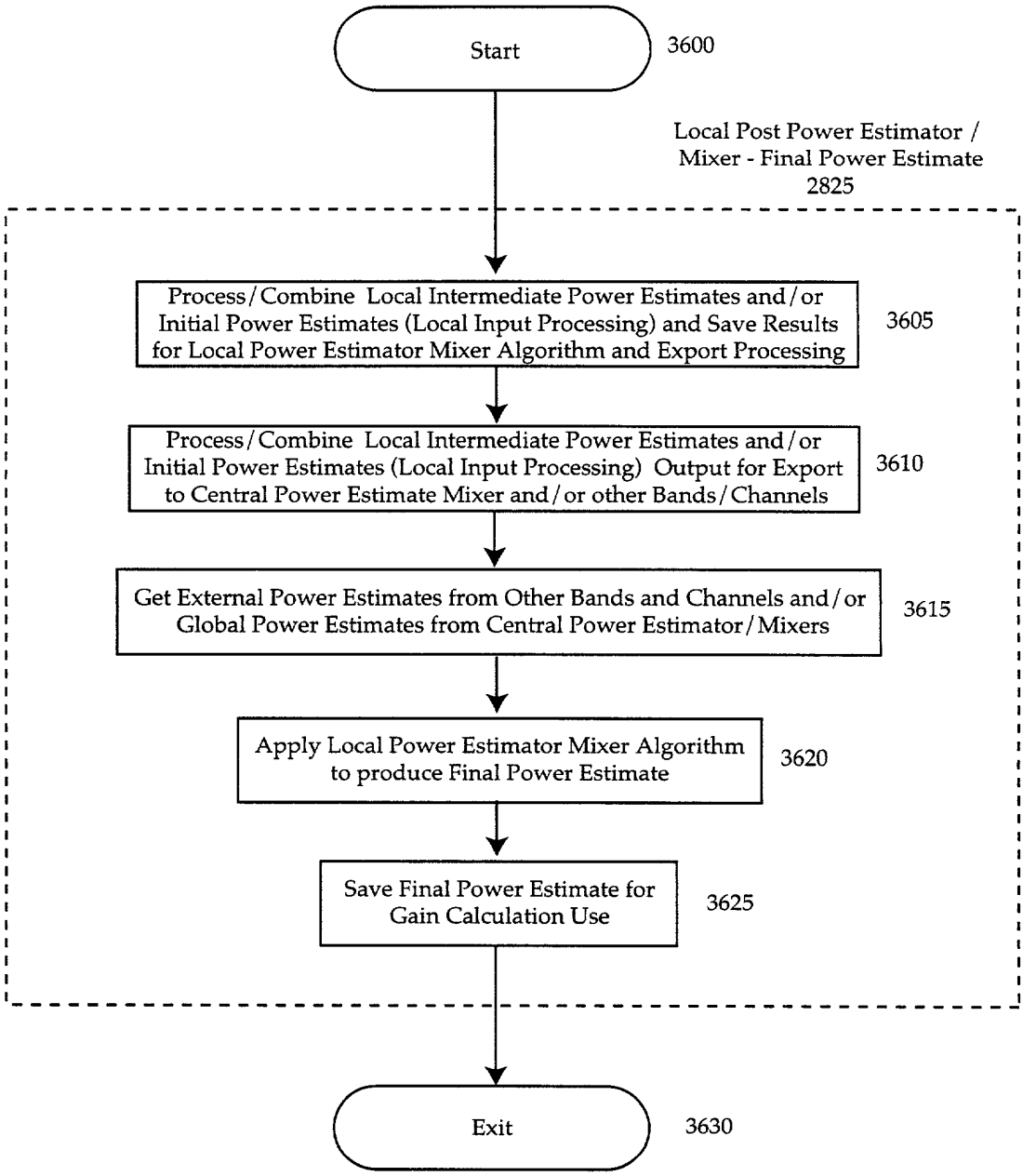

Start
3600
Local Post Power Estimator / Mixer - Final Power Estimate 2825
Process/Combine Local Intermediate Power Estimates and/or Initial Power Estimates (Local Input Processing) and Save Results for Local Power Estimator Mixer Algorithm and Export Processing
3605
Process/Combine Local Intermediate Power Estimates and/or Initial Power Estimates (Local Input Processing) Output for Export to Central Power Estimate Mixer and/or other Bands/Channels
3610
Get External Power Estimates from Other Bands and Channels and/or Global Power Estimates from Central Power Estimator/Mixers
3615
Apply Local Power Estimator Mixer Algorithm to produce Final Power Estimate
3620
Save Final Power Estimate for Gain Calculation Use
3625
Exit
3630

FIG. 36

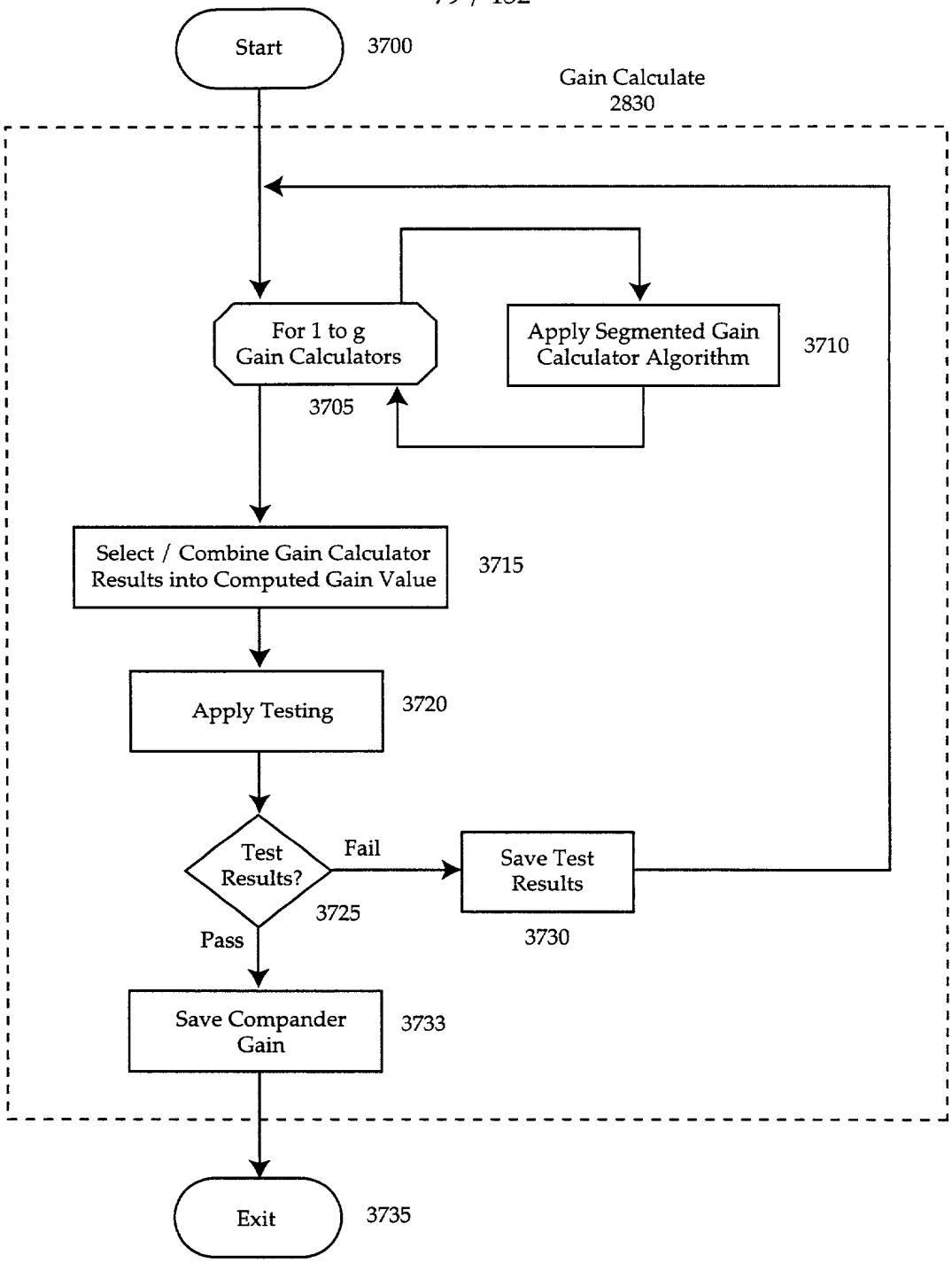

Start
3700
Gain Calculate
2830
For 1 to g
Gain Calculators
3705
Apply Segmented Gain
Calculator Algorithm
3710
Select / Combine Gain Calculator
Results into Computed Gain Value
3715
Apply Testing
3720
Test
Results?
3725
Fail
Save Test
Results
3730
Pass
Save Compander
Gain
3733
Exit
3735

FIG. 37A

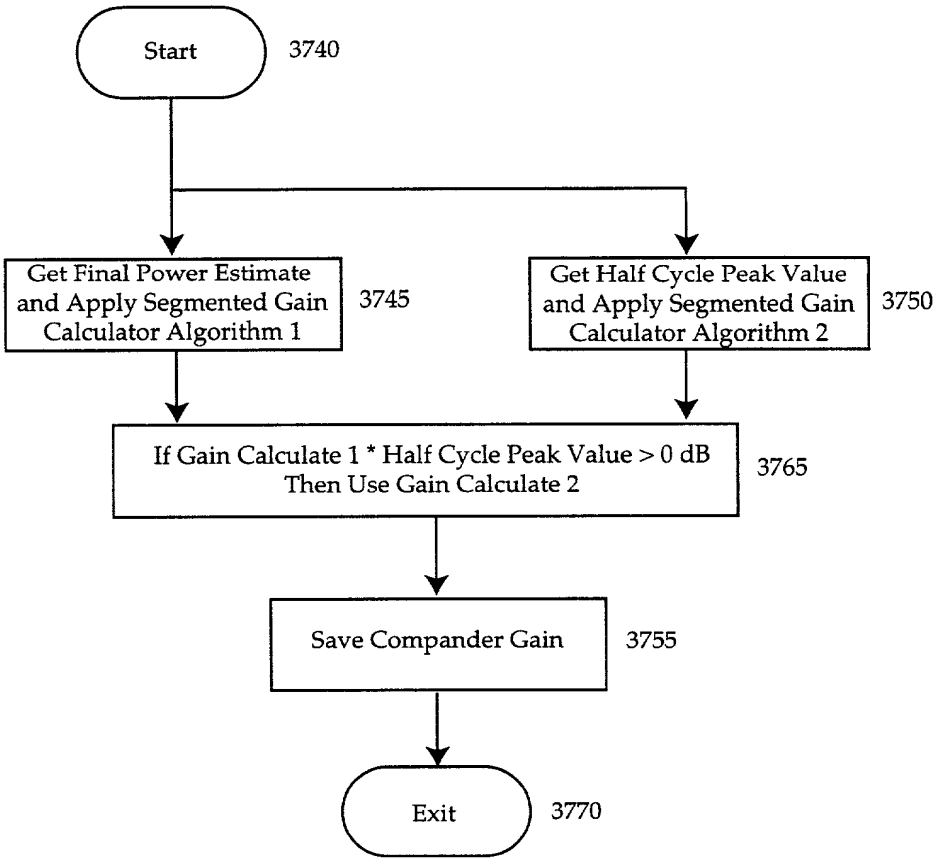

Start
3740
Get Final Power Estimate and Apply Segmented Gain Calculator Algorithm 1
3745
Get Half Cycle Peak Value and Apply Segmented Gain Calculator Algorithm 2
3750
If Gain Calculate 1 * Half Cycle Peak Value > 0 dB Then Use Gain Calculate 2
3765
Save Compander Gain
3755
Exit
3770

FIG. 37B

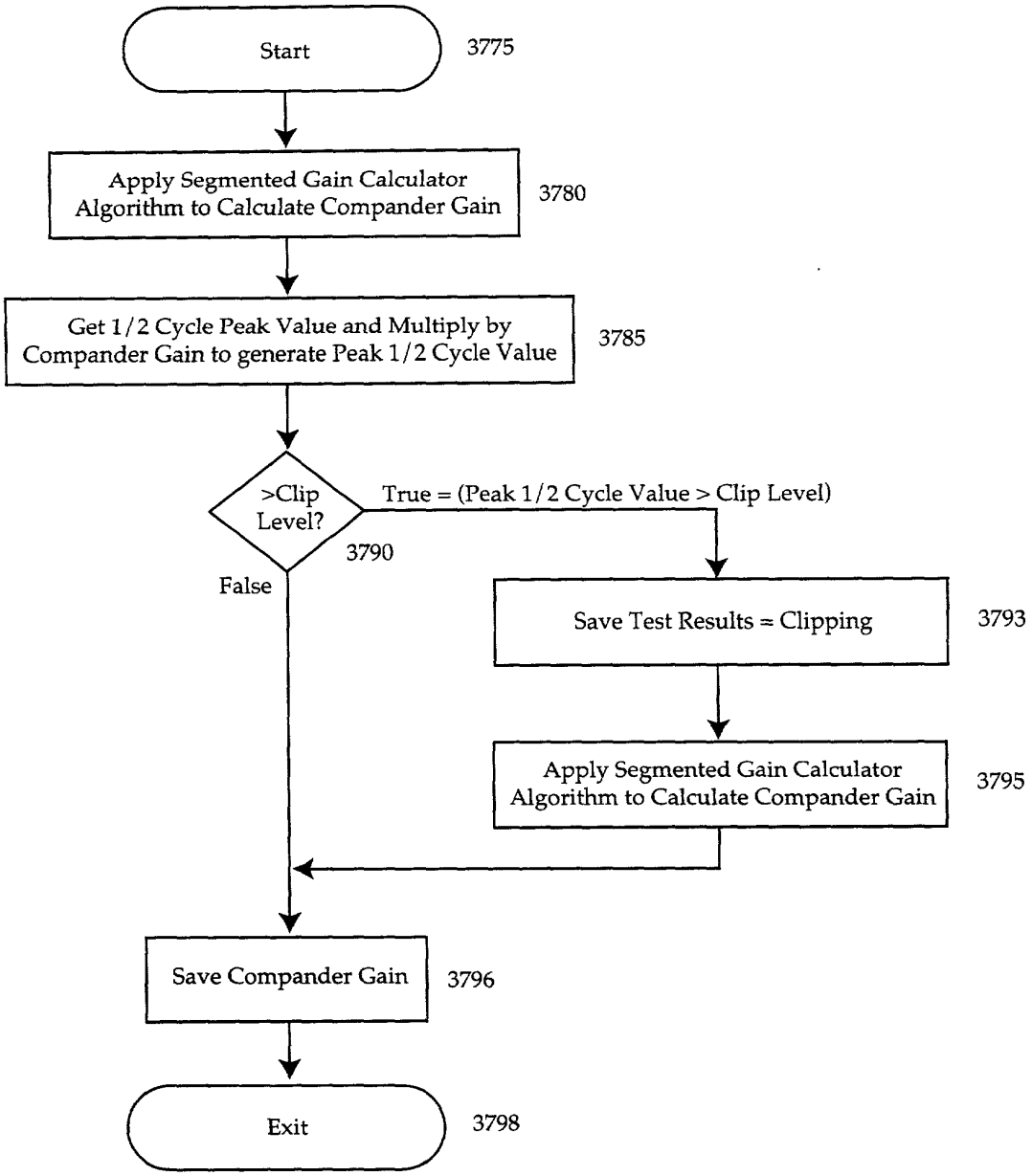

Start
3775
Apply Segmented Gain Calculator Algorithm to Calculate Compander Gain
3780
Get 1/2 Cycle Peak Value and Multiply by Compander Gain to generate Peak 1/2 Cycle Value
3785
>Clip Level?
3790
True = (Peak 1/2 Cycle Value > Clip Level)
False
Save Test Results = Clipping
3793
Apply Segmented Gain Calculator Algorithm to Calculate Compander Gain
3795
Save Compander Gain
3796
Exit
3798

FIG. 37C

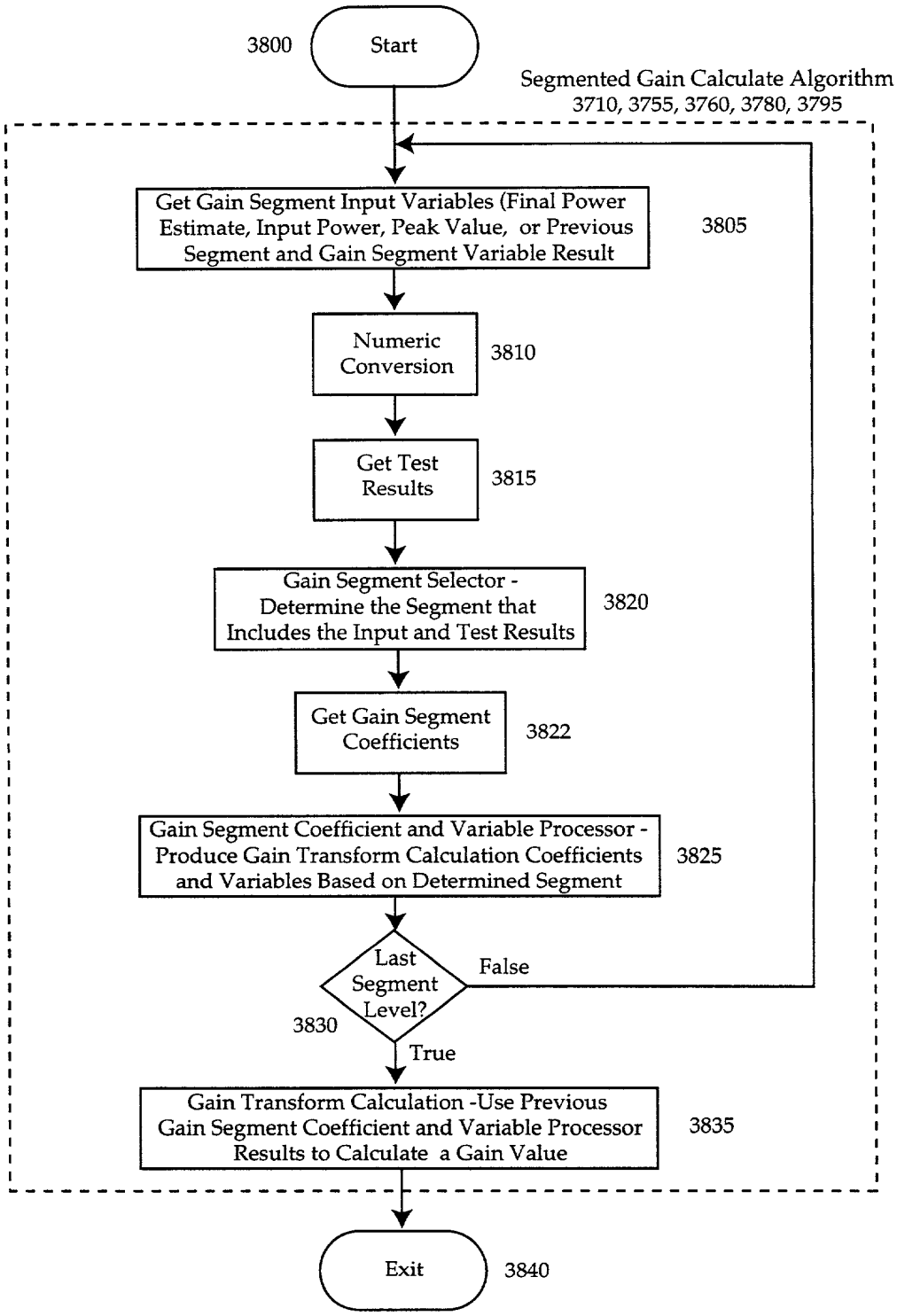

3800
Start
Segmented Gain Calculate Algorithm
3710, 3755, 3760, 3780, 3795
Get Gain Segment Input Variables (Final Power Estimate, Input Power, Peak Value, or Previous Segment and Gain Segment Variable Result
3805
Numeric Conversion
3810
Get Test Results
3815
Gain Segment Selector - Determine the Segment that Includes the Input and Test Results
3820
Get Gain Segment Coefficients
3822
Gain Segment Coefficient and Variable Processor - Produce Gain Transform Calculation Coefficients and Variables Based on Determined Segment
3825
Last Segment Level?
3830
False
True
Gain Transform Calculation -Use Previous Gain Segment Coefficient and Variable Processor Results to Calculate a Gain Value
3835
Exit
3840

FIG. 38

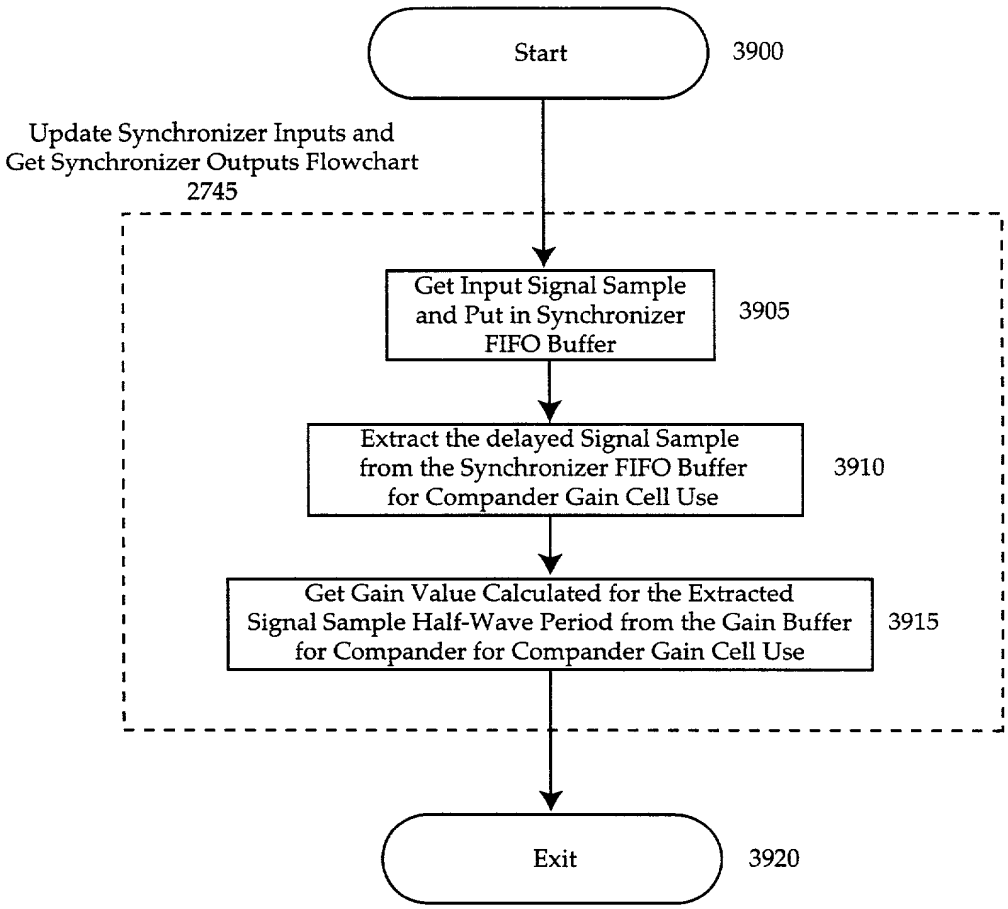

Start
3900
Update Synchronizer Inputs and Get Synchronizer Outputs Flowchart 2745
Get Input Signal Sample and Put in Synchronizer FIFO Buffer
3905
Extract the delayed Signal Sample from the Synchronizer FIFO Buffer for Compander Gain Cell Use
3910
Get Gain Value Calculated for the Extracted Signal Sample Half-Wave Period from the Gain Buffer for Compander for Compander Gain Cell Use
3915
Exit
3920

FIG. 39

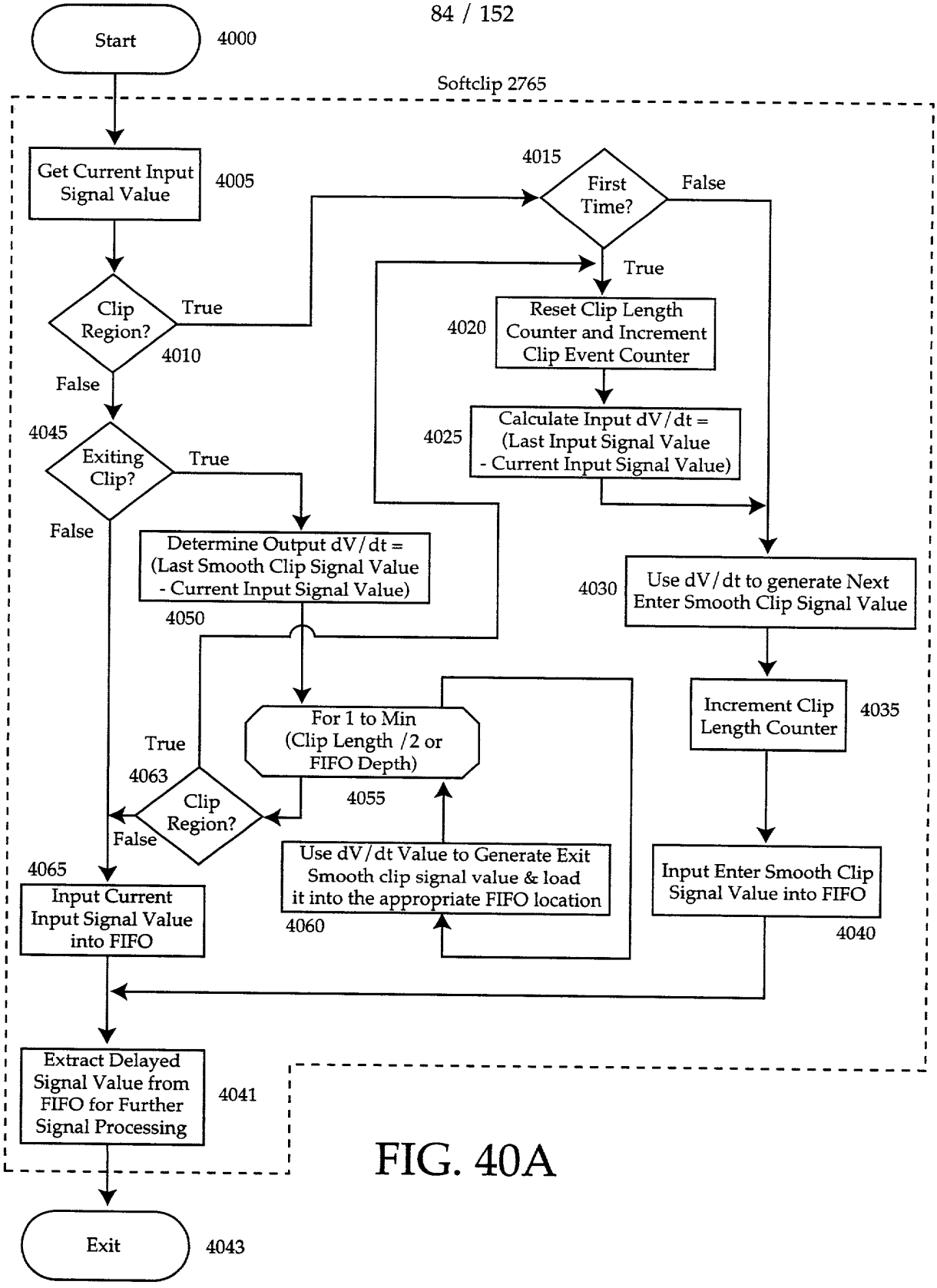

Start
4000
Softclip 2765
Get Current Input Signal Value
4005
Clip Region?
4010
True
False
4015
First Time?
False
True
4020
Reset Clip Length Counter and Increment Clip Event Counter
4025
Calculate Input dV/dt = (Last Input Signal Value - Current Input Signal Value)
4045
Exiting Clip?
True
False
Determine Output dV/dt = (Last Smooth Clip Signal Value - Current Input Signal Value)
4050
4030
Use dV/dt to generate Next Enter Smooth Clip Signal Value
Increment Clip Length Counter
4035
For 1 to Min (Clip Length /2 or FIFO Depth)
4055
True
4063
Clip Region?
False
Use dV/dt Value to Generate Exit Smooth clip signal value & load it into the appropriate FIFO location
4060
Input Enter Smooth Clip Signal Value into FIFO
4040
4065
Input Current Input Signal Value into FIFO
Extract Delayed Signal Value from FIFO for Further Signal Processing
4041
Exit
4043

FIG. 40A

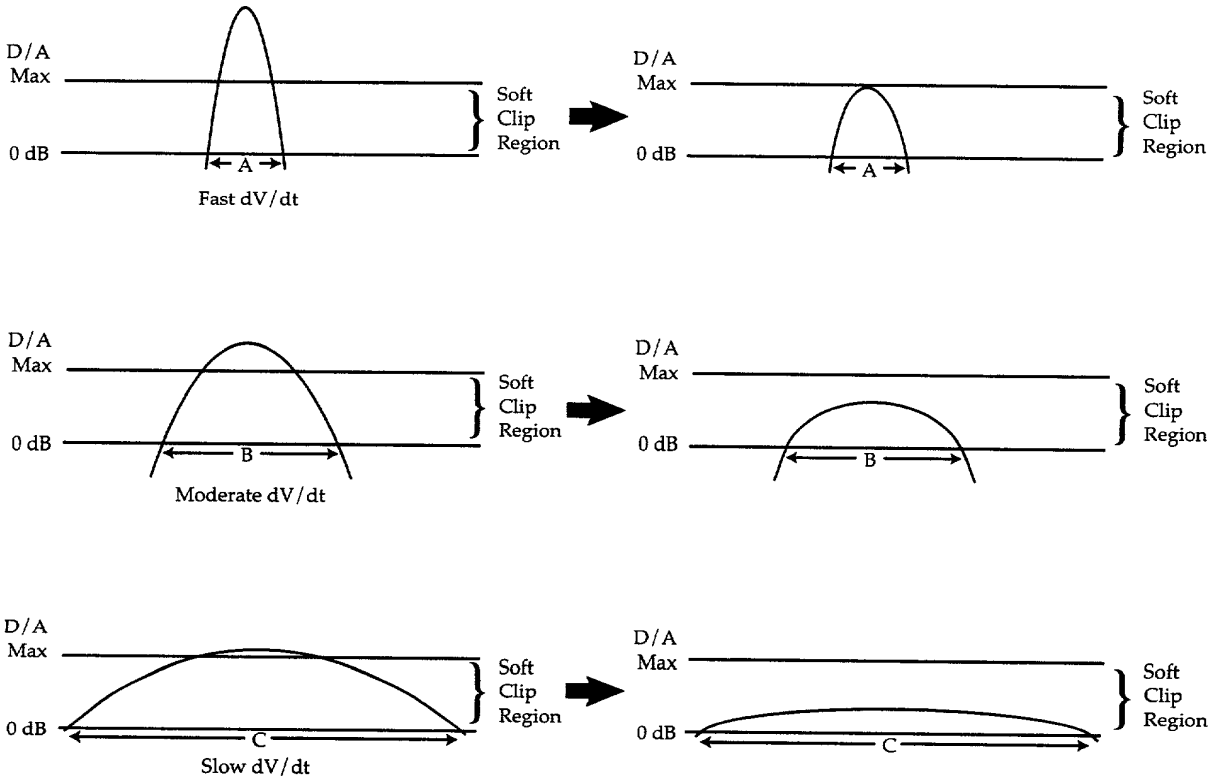

D/A
Max
0 dB
A
Soft
Clip
Region
Fast dV/dt
D/A
Max
0 dB
A
Soft
Clip
Region
D/A
Max
0 dB
B
Soft
Clip
Region
Moderate dV/dt
D/A
Max
0 dB
B
Soft
Clip
Region
D/A
Max
0 dB
C
Soft
Clip
Region
Slow dV/dt
D/A
Max
0 dB
C
Soft
Clip
Region

FIG. 40B

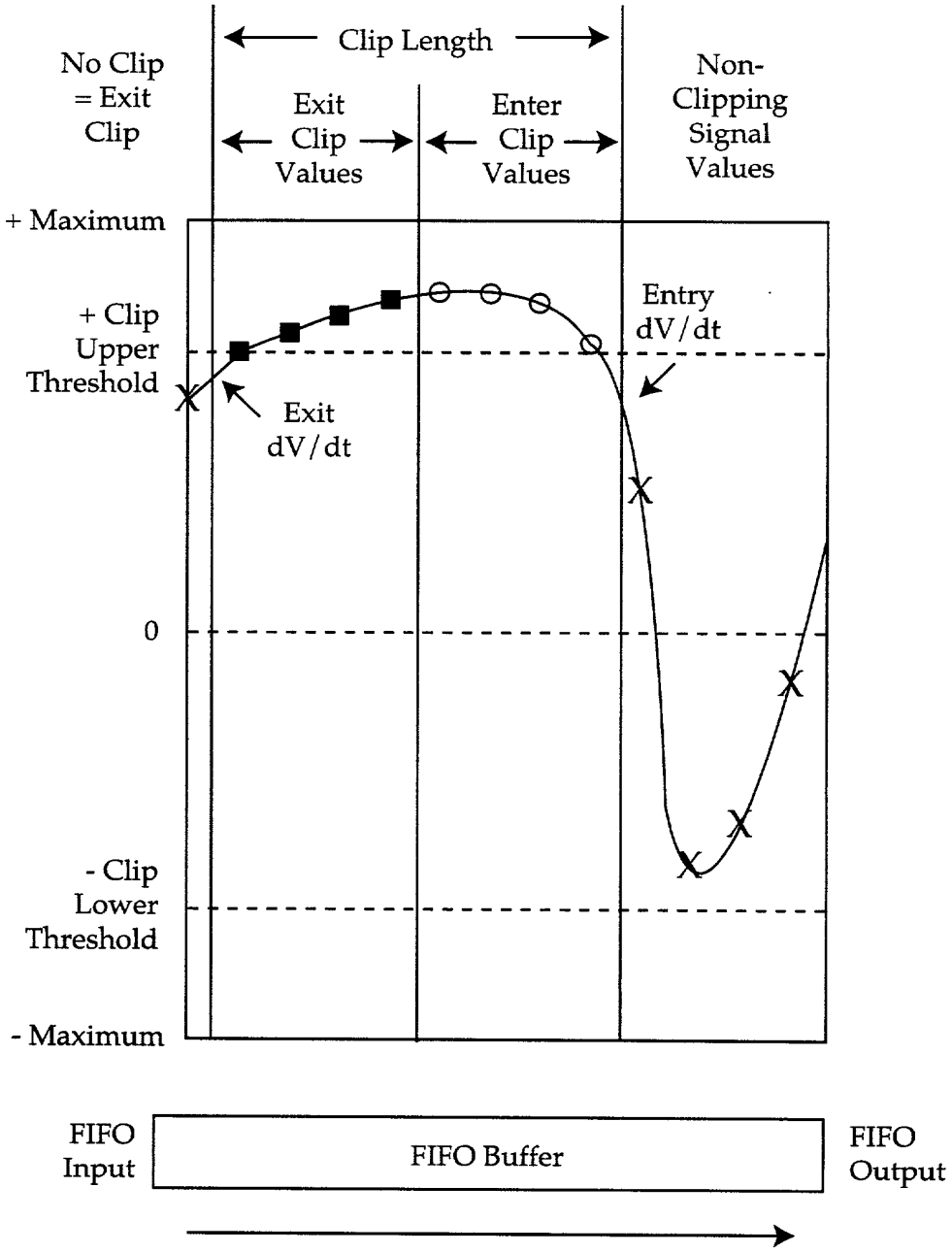

Clip Length
No Clip = Exit Clip
Exit Clip Values
Enter Clip Values
Non-Clipping Signal Values
+ Maximum
+ Clip Upper Threshold
Entry dV/dt
Exit dV/dt
0
- Clip Lower Threshold
- Maximum
FIFO Input
FIFO Buffer
FIFO Output

FIG. 40C

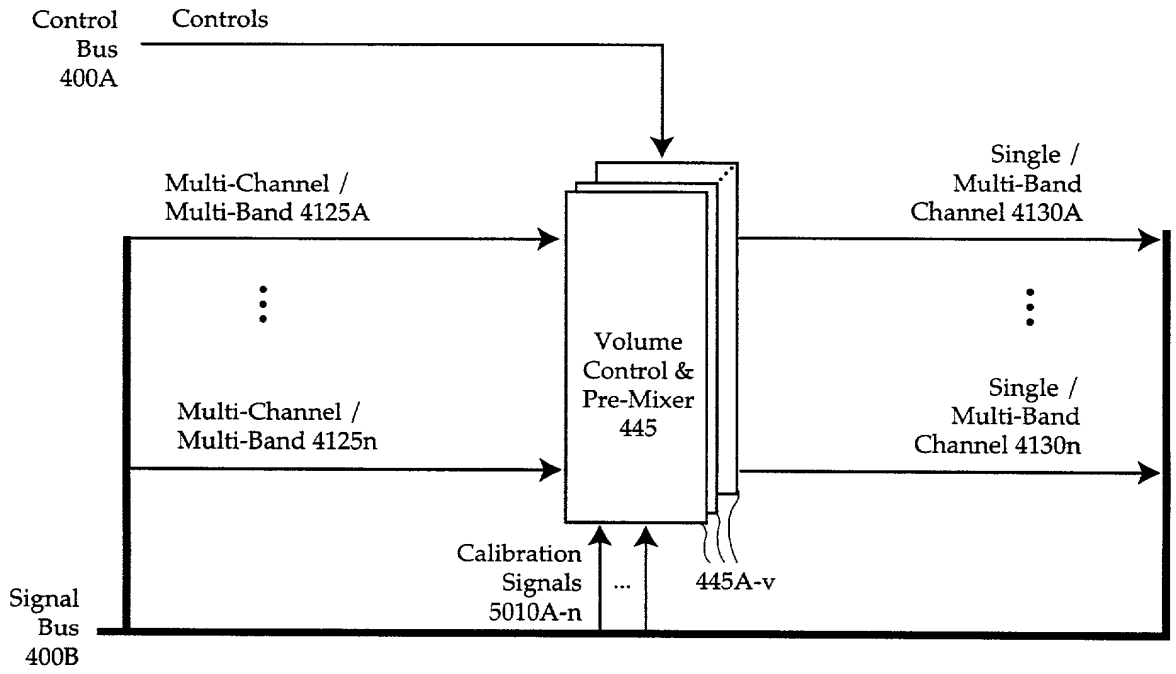

Control
Bus
400A
Controls
Multi-Channel /
Multi-Band 4125A
Multi-Channel /
Multi-Band 4125n
Volume
Control &
Pre-Mixer
445
Single /
Multi-Band
Channel 4130A
Single /
Multi-Band
Channel 4130n
Calibration
Signals
5010A-n
...
445A-v
Signal
Bus
400B

FIG. 41A

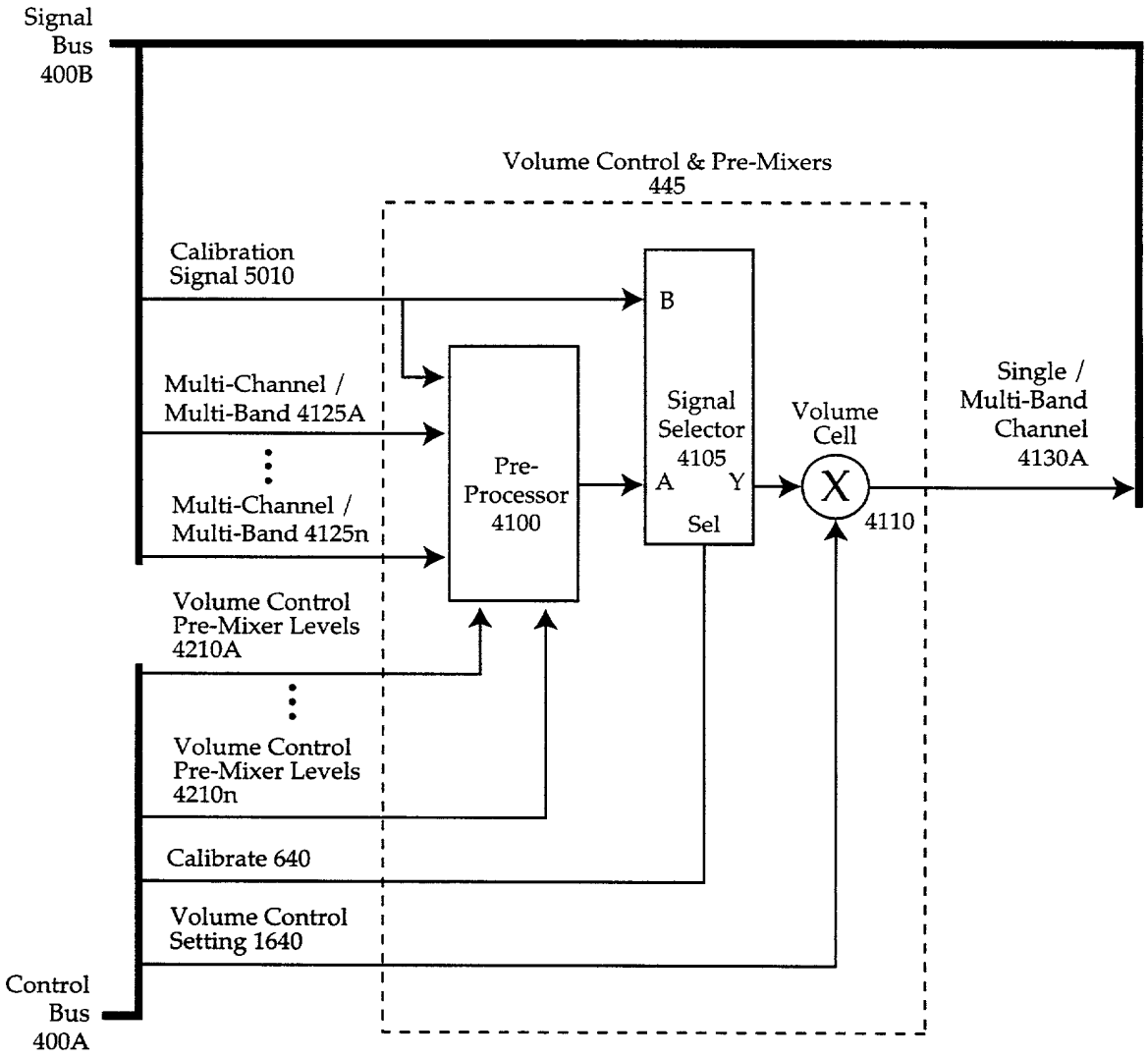
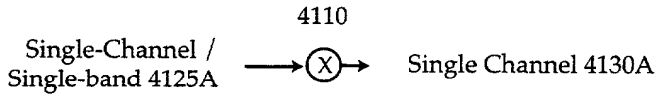
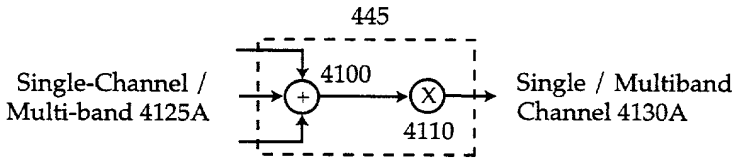

Signal
Bus
400B
Volume Control & Pre-Mixers
445
Calibration
Signal 5010
Multi-Channel /
Multi-Band 4125A
Multi-Channel /
Multi-Band 4125n
Pre-
Processor
4100
B
Signal
Selector
4105
A
Y
Sel
Volume
Cell
X
4110
Single /
Multi-Band
Channel
4130A
Volume Control
Pre-Mixer Levels
4210A
Volume Control
Pre-Mixer Levels
4210n
Calibrate 640
Volume Control
Setting 1640
Control
Bus
400A

FIG. 41B



1 Band/Channel + Volume Control

FIG. 42A



3 Band/Channel + PreMix / Volume Control

FIG. 42B

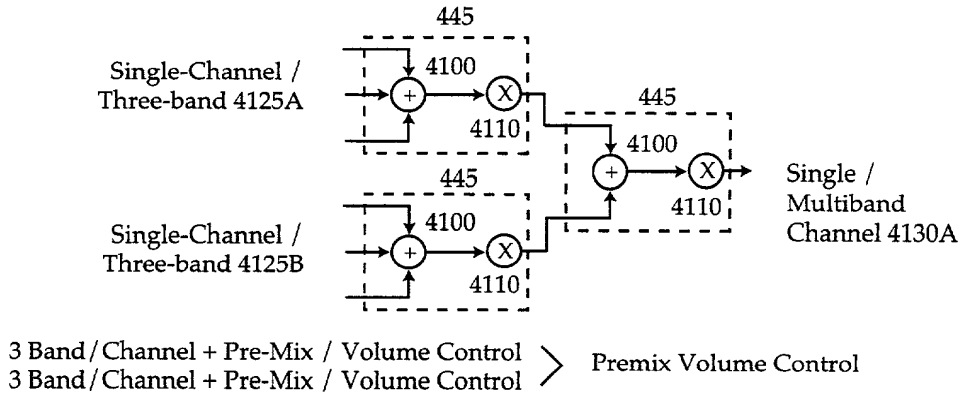


FIG. 42C

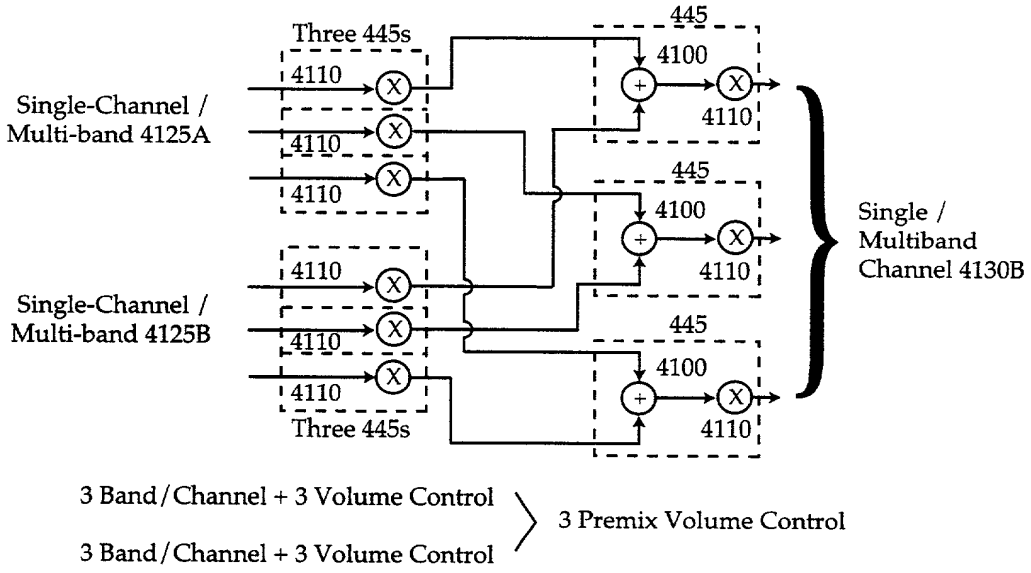


FIG. 42D

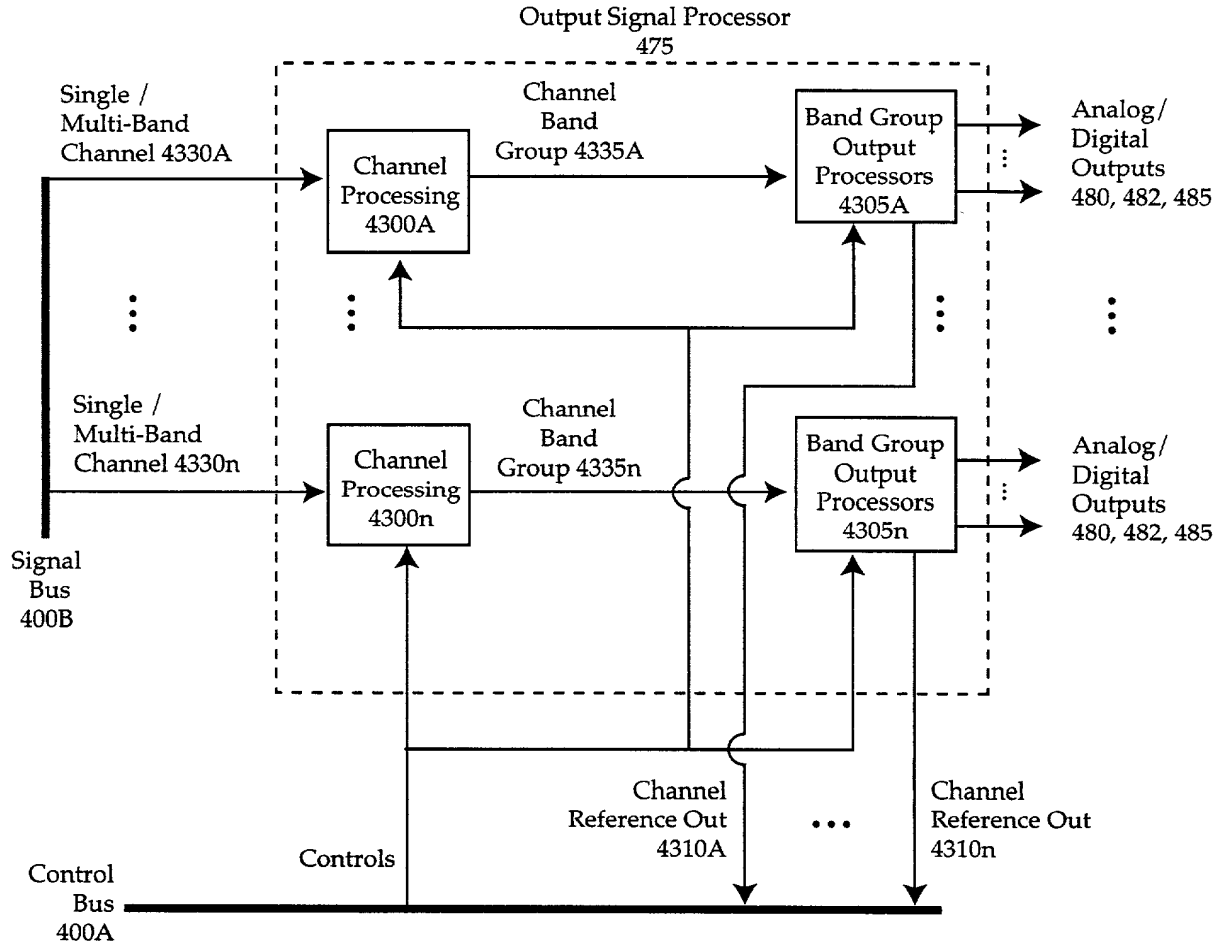

Output Signal Processor
475
Single /
Multi-Band
Channel 4330A
Channel
Processing
4300A
Channel
Band
Group 4335A
Band Group
Output
Processors
4305A
Analog/
Digital
Outputs
480, 482, 485
Single /
Multi-Band
Channel 4330n
Channel
Processing
4300n
Channel
Band
Group 4335n
Band Group
Output
Processors
4305n
Analog/
Digital
Outputs
480, 482, 485
Signal
Bus
400B
Channel
Reference Out
4310A
Channel
Reference Out
4310n
Controls
Control
Bus
400A

FIG. 43A

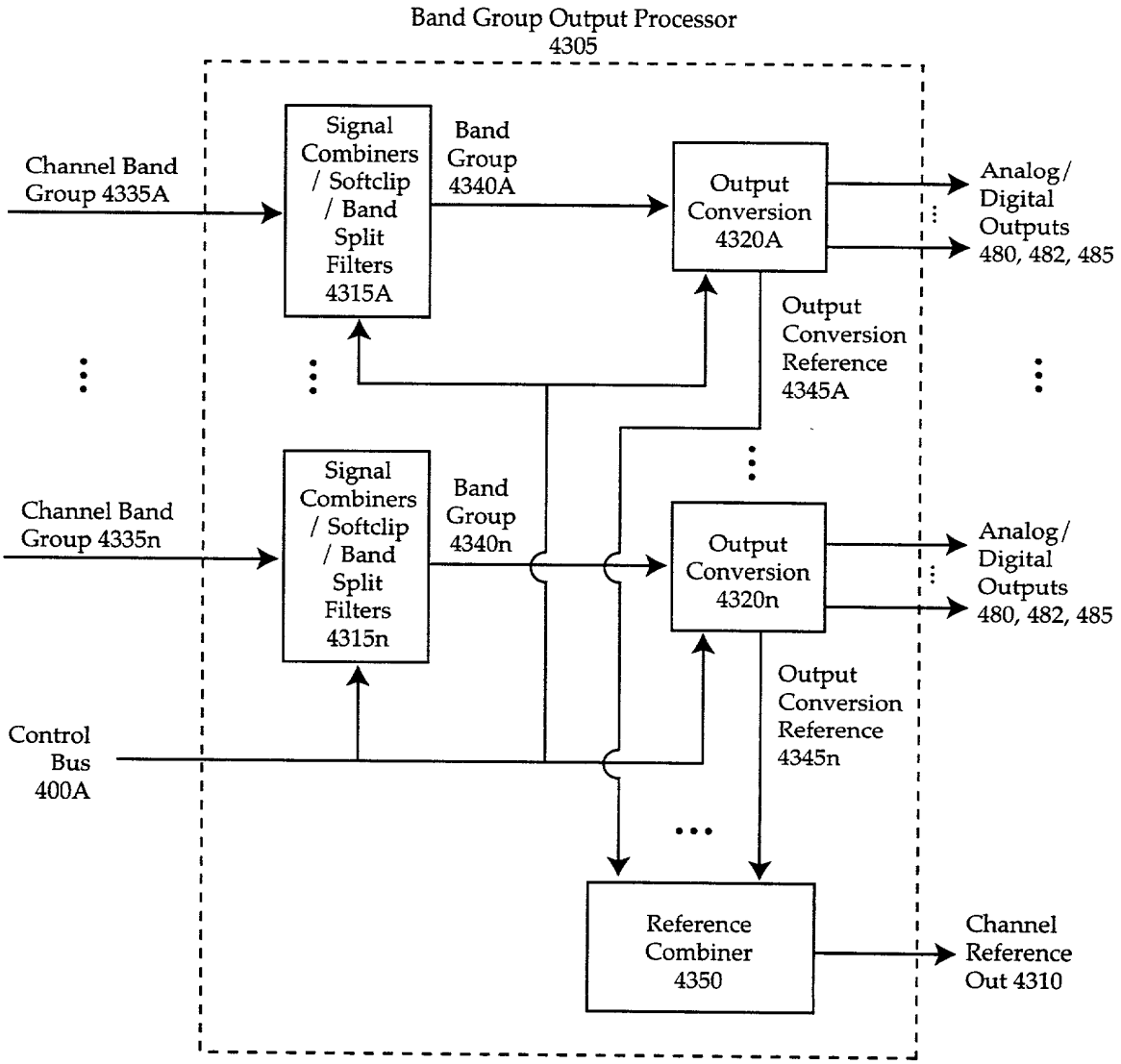

Band Group Output Processor
4305
Channel Band Group 4335A
Signal Combiners / Softclip / Band Split Filters 4315A
Band Group 4340A
Output Conversion 4320A
Analog/ Digital Outputs 480, 482, 485
Output Conversion Reference 4345A
Channel Band Group 4335n
Signal Combiners / Softclip / Band Split Filters 4315n
Band Group 4340n
Output Conversion 4320n
Analog/ Digital Outputs 480, 482, 485
Output Conversion Reference 4345n
Control Bus 400A
Reference Combiner 4350
Channel Reference Out 4310

FIG. 43B

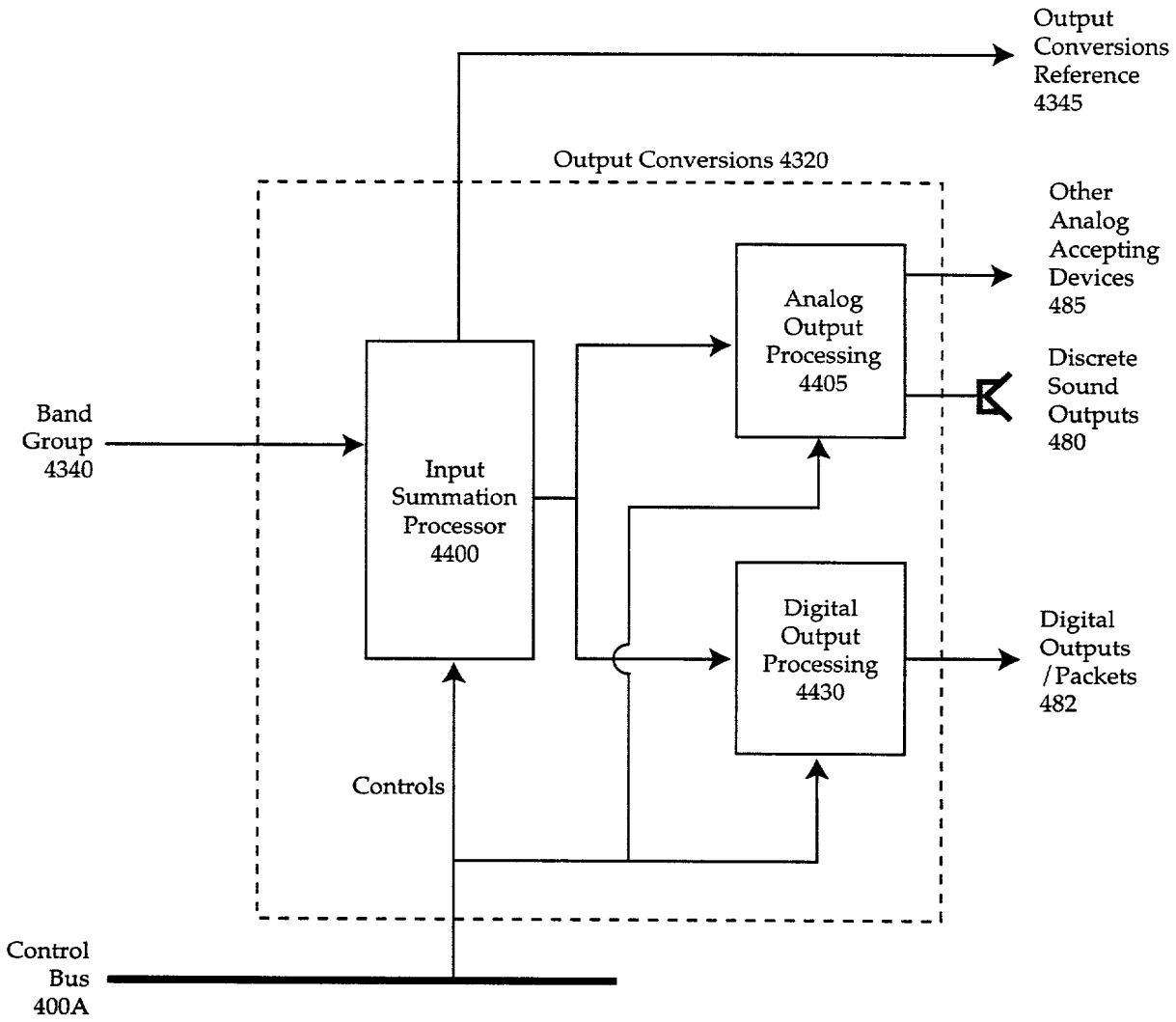

Output
Conversions
Reference
4345
Output Conversions 4320
Other
Analog
Accepting
Devices
485
Analog
Output
Processing
4405
Discrete
Sound
Outputs
480
Band
Group
4340
Input
Summation
Processor
4400
Digital
Output
Processing
4430
Digital
Outputs
/Packets
482
Controls
Control
Bus
400A

FIG. 44

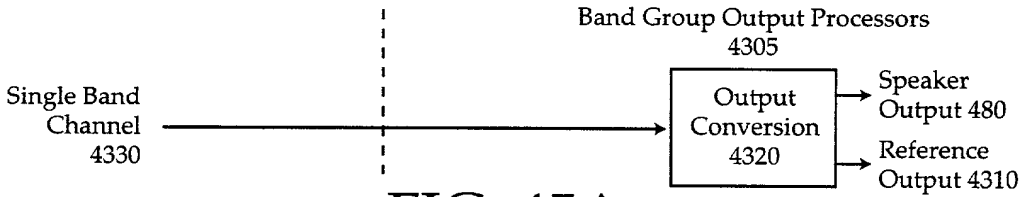


FIG. 45A

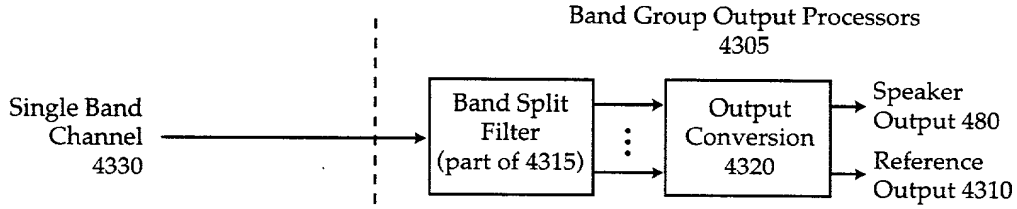


FIG. 45B

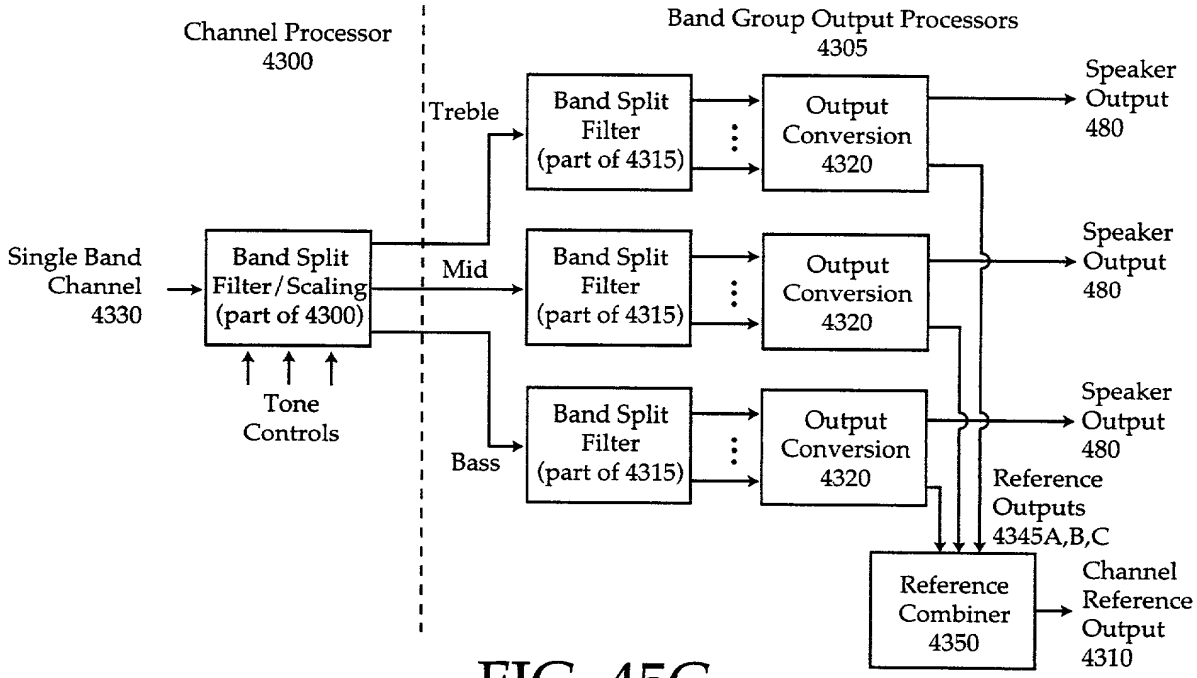


FIG. 45C

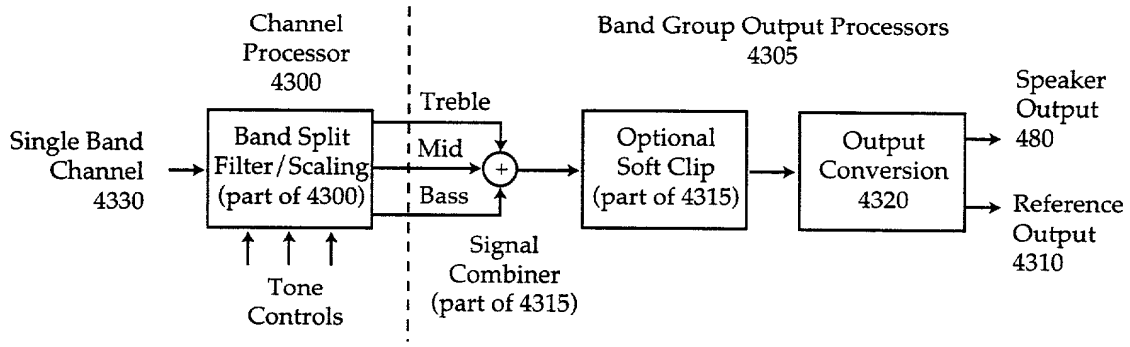


FIG. 45D

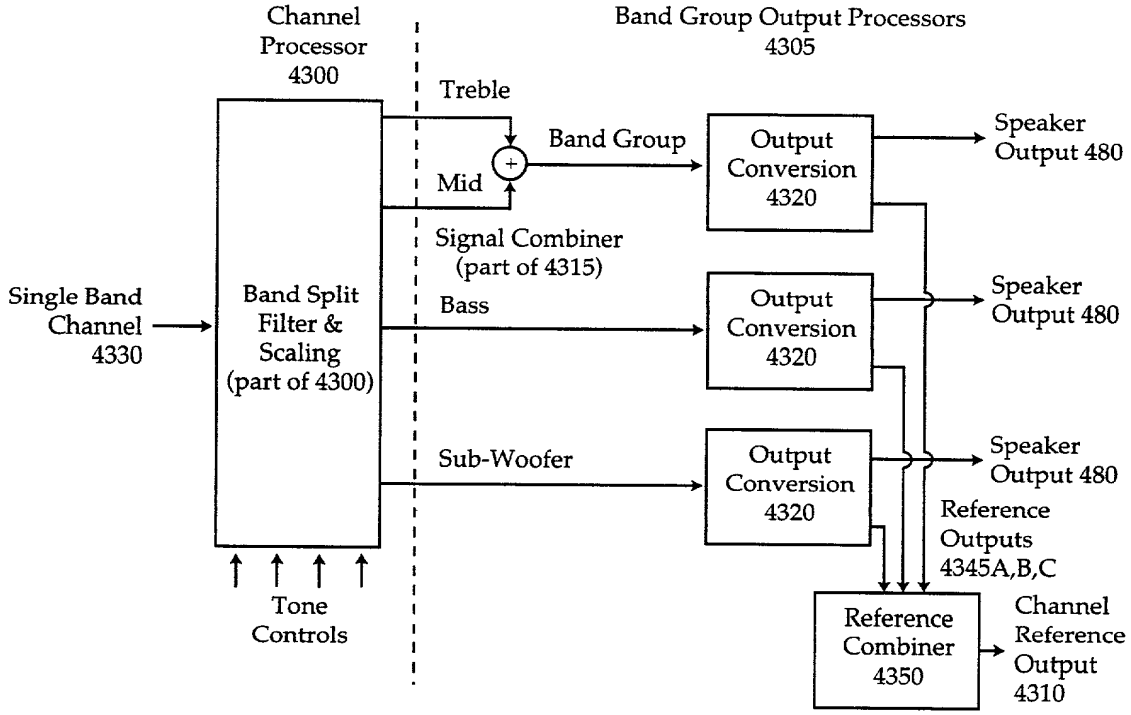


FIG. 45E

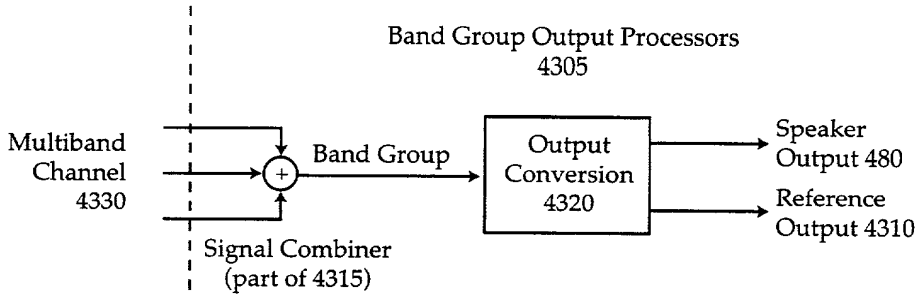


FIG. 45F

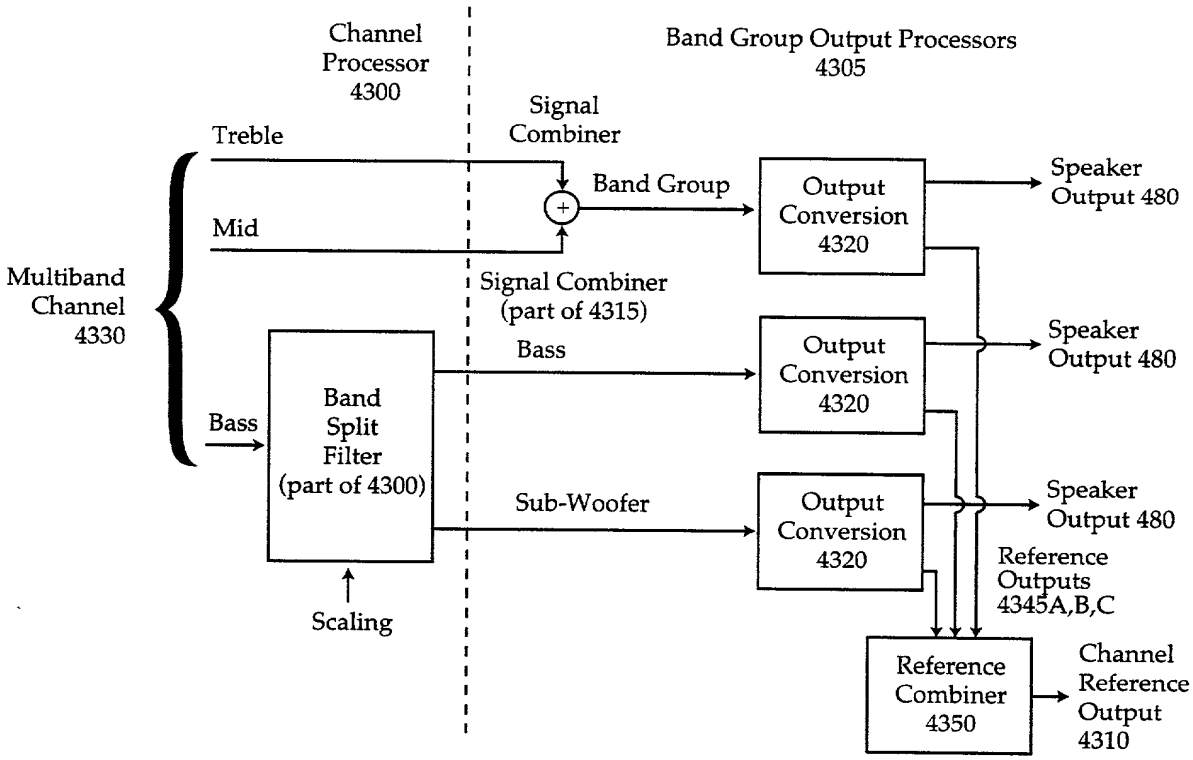


FIG. 45G

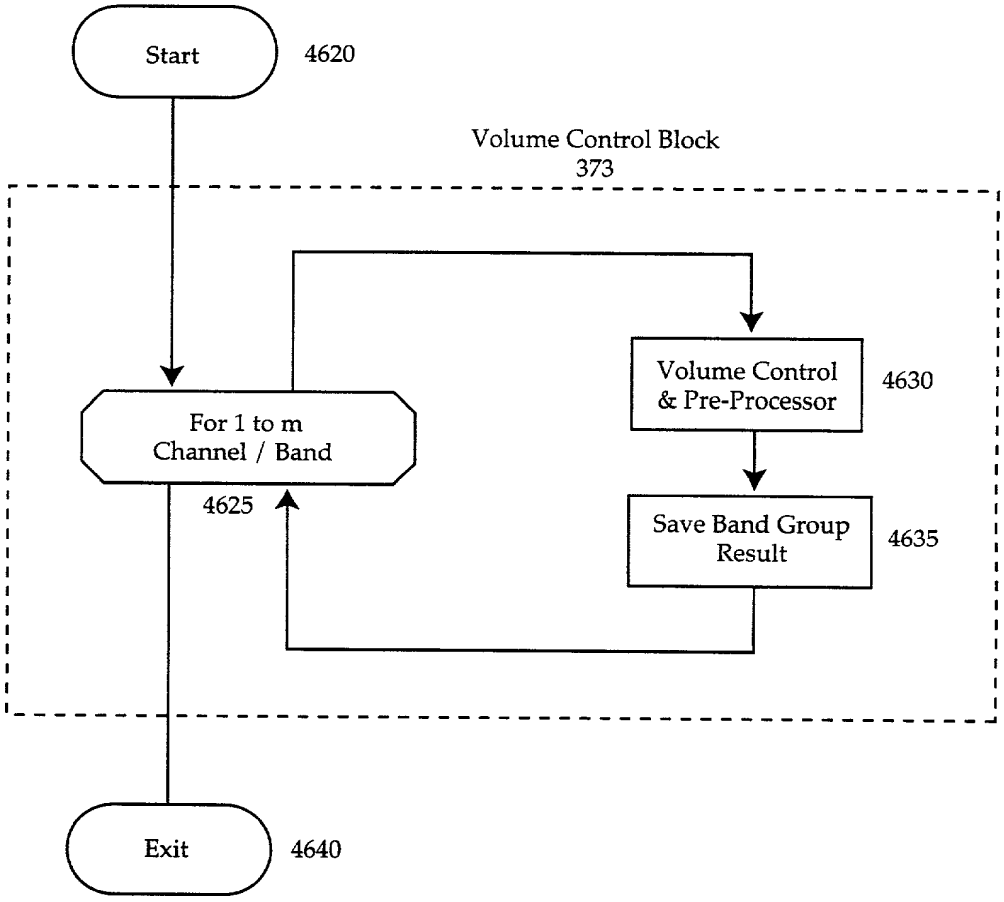

Start
4620
Volume Control Block
373
Volume Control
& Pre-Processor
4630
For 1 to m
Channel / Band
4625
Save Band Group
Result
4635
Exit
4640

FIG. 46

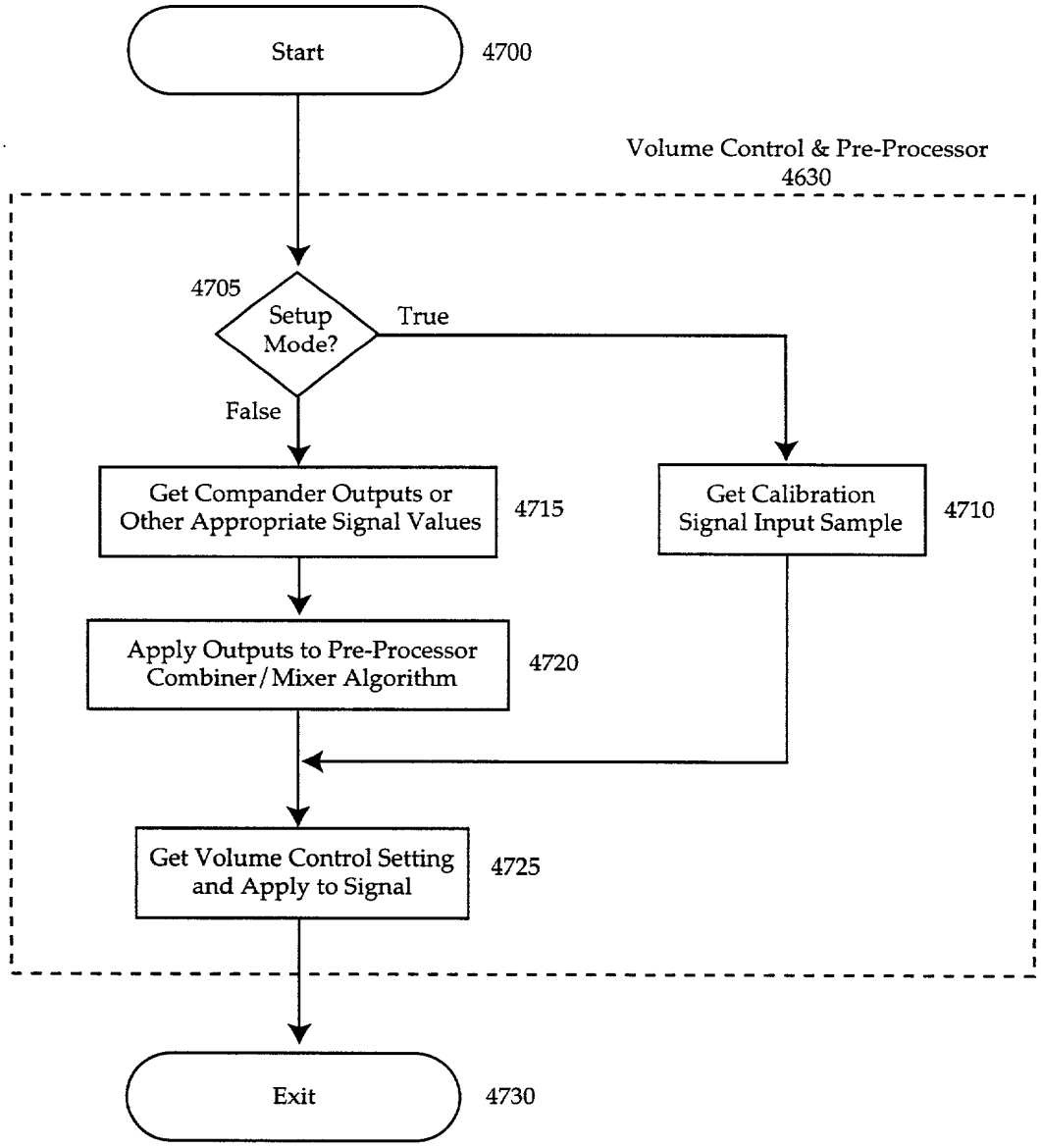

Start
4700
Volume Control & Pre-Processor
4630
4705
Setup Mode?
True
False
Get Compander Outputs or Other Appropriate Signal Values
4715
Get Calibration Signal Input Sample
4710
Apply Outputs to Pre-Processor Combiner/Mixer Algorithm
4720
Get Volume Control Setting and Apply to Signal
4725
Exit
4730

FIG. 47

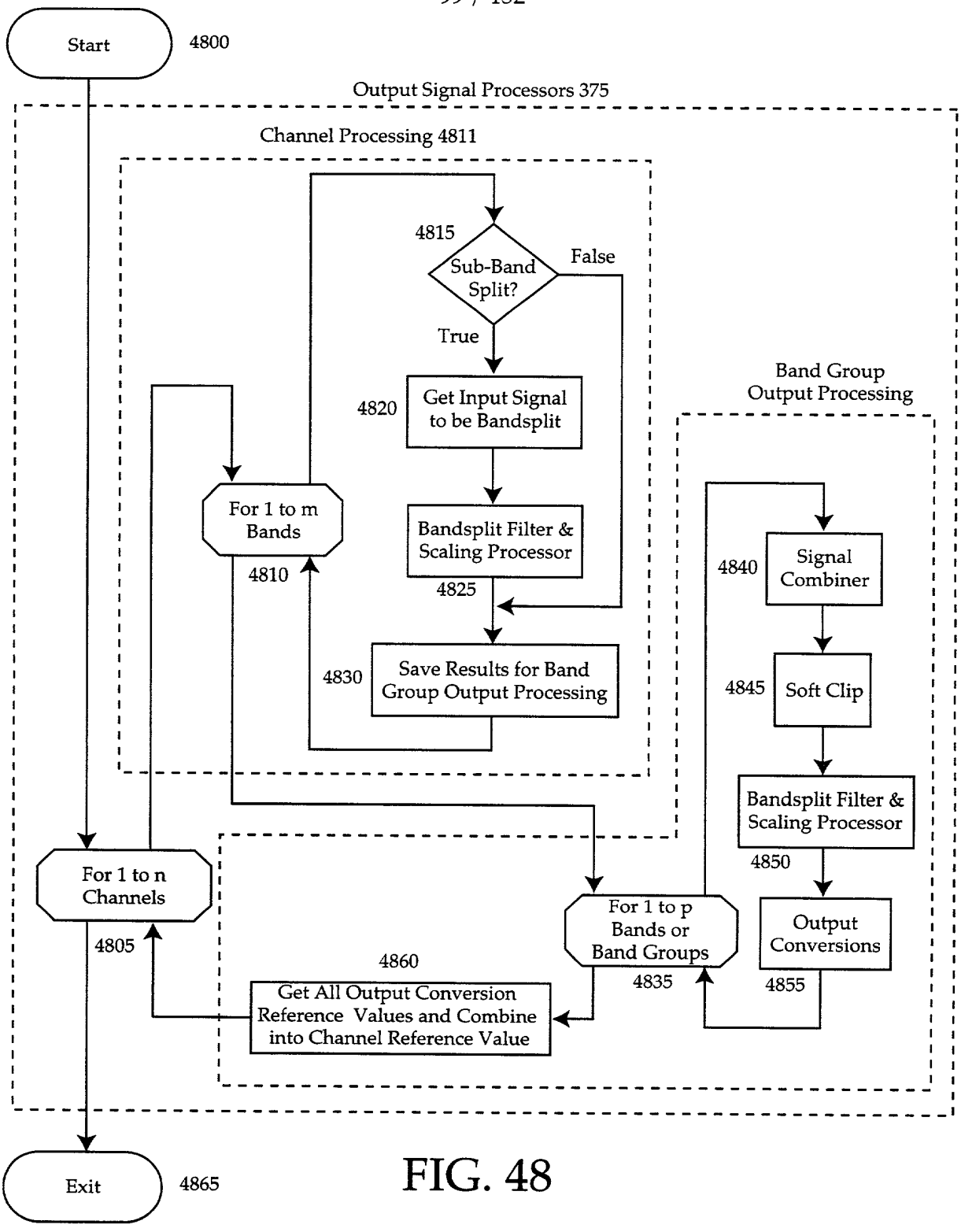

Start
4800
Output Signal Processors 375
Channel Processing 4811
4815
Sub-Band Split?
False
True
4820
Get Input Signal to be Bandsplit
Bandsplit Filter & Scaling Processor
4825
4830
Save Results for Band Group Output Processing
For 1 to m Bands
4810
Band Group Output Processing
4840
Signal Combiner
4845
Soft Clip
Bandsplit Filter & Scaling Processor
4850
For 1 to n Channels
4805
For 1 to p Bands or Band Groups
4835
Output Conversions
4855
4860
Get All Output Conversion Reference Values and Combine into Channel Reference Value
Exit
4865

FIG. 48

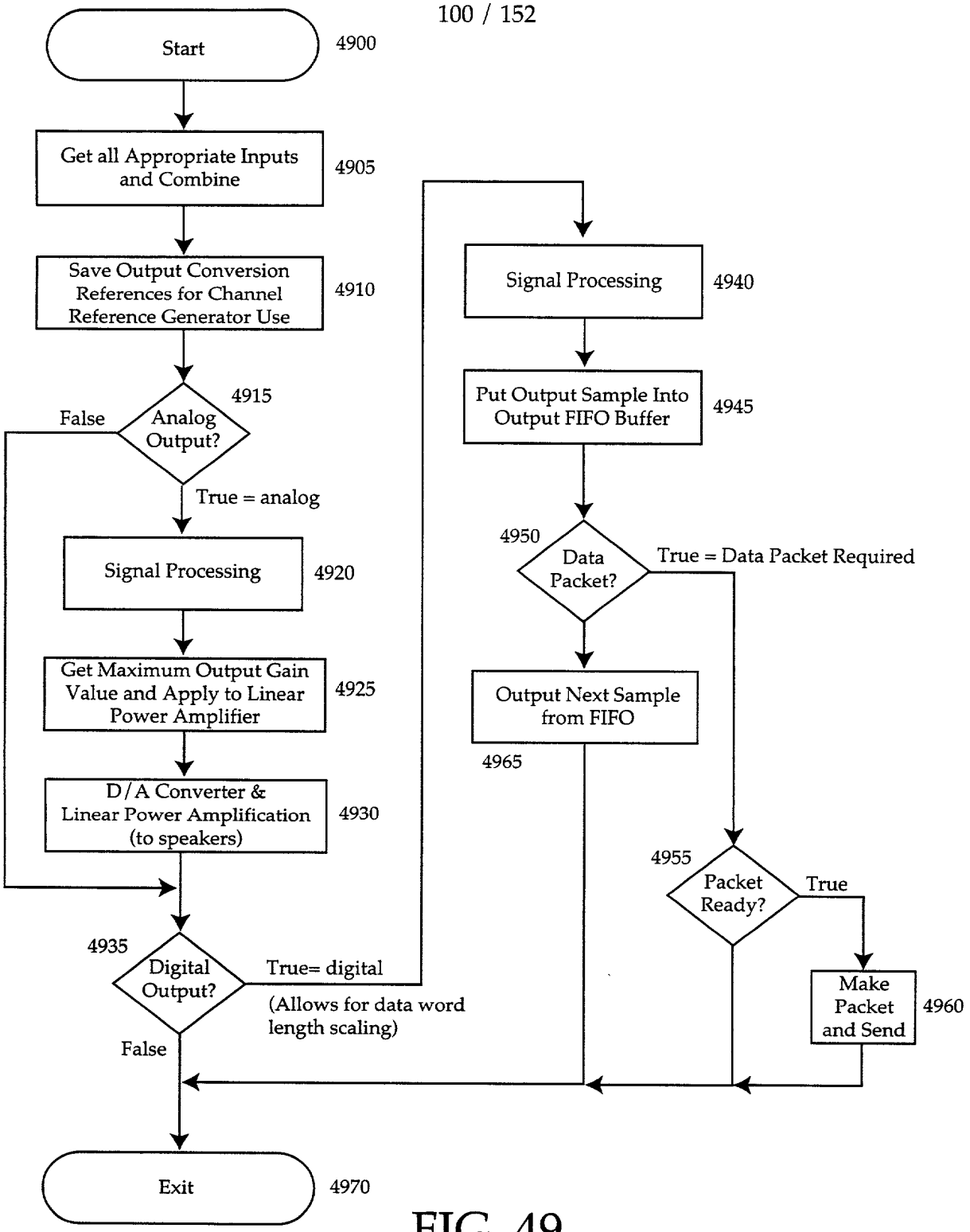

Start
4900
Get all Appropriate Inputs and Combine
4905
Save Output Conversion References for Channel Reference Generator Use
4910
Analog Output?
4915
False
True = analog
Signal Processing
4920
Get Maximum Output Gain Value and Apply to Linear Power Amplifier
4925
D/A Converter & Linear Power Amplification (to speakers)
4930
Digital Output?
4935
True= digital
(Allows for data word length scaling)
False
Signal Processing
4940
Put Output Sample Into Output FIFO Buffer
4945
Data Packet?
4950
True = Data Packet Required
Output Next Sample from FIFO
4965
Packet Ready?
4955
True
Make Packet and Send
4960
Exit
4970

FIG. 49

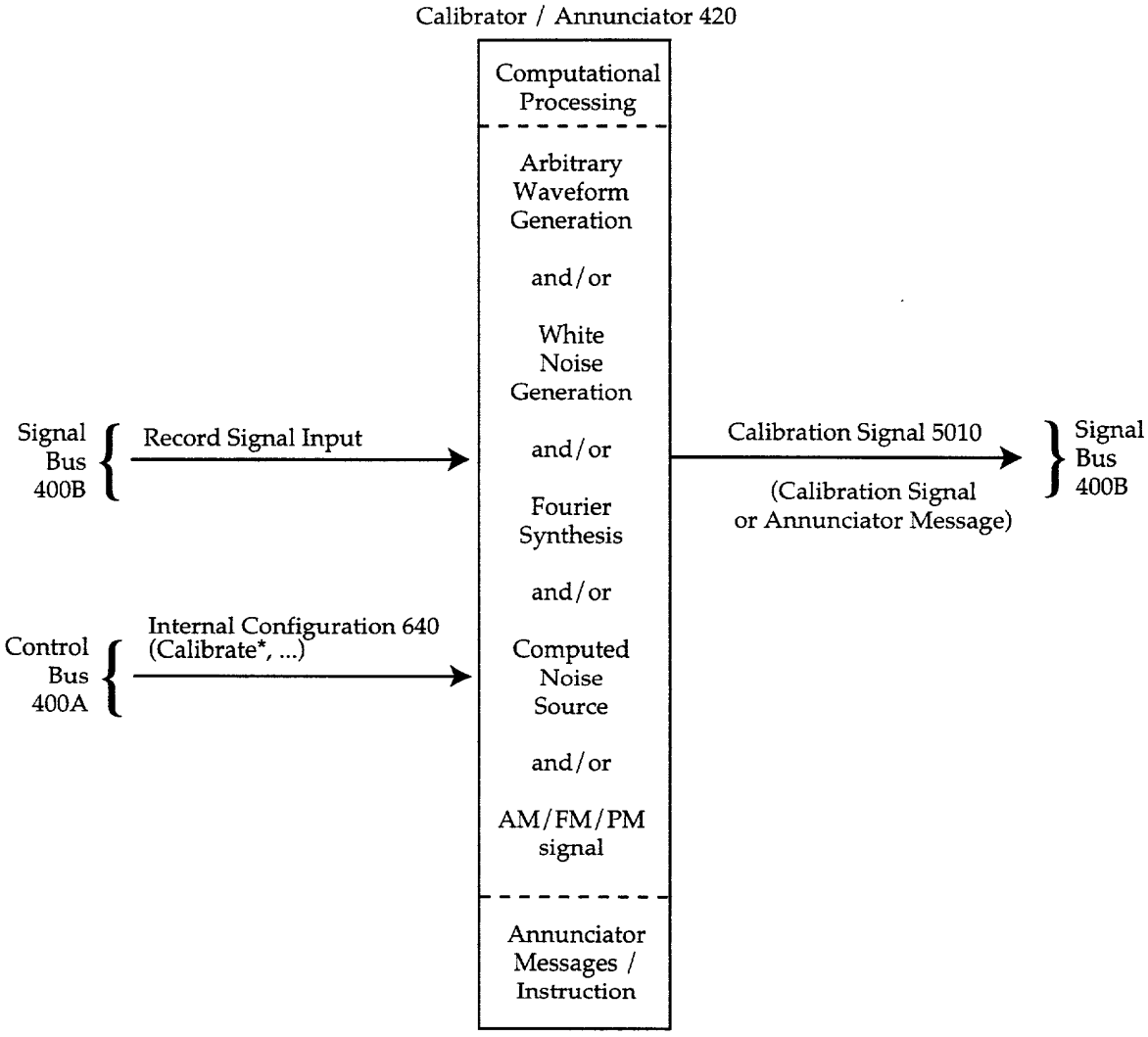

Calibrator / Annunciator 420
Computational Processing
Arbitrary Waveform Generation
and/or
White Noise Generation
and/or
Fourier Synthesis
and/or
Computed Noise Source
and/or
AM/FM/PM signal
Annunciator Messages / Instruction
Signal Bus 400B
Record Signal Input
Control Bus 400A
Internal Configuration 640 (Calibrate*, ...)
Calibration Signal 5010
(Calibration Signal or Annunciator Message)
Signal Bus 400B

FIG. 50

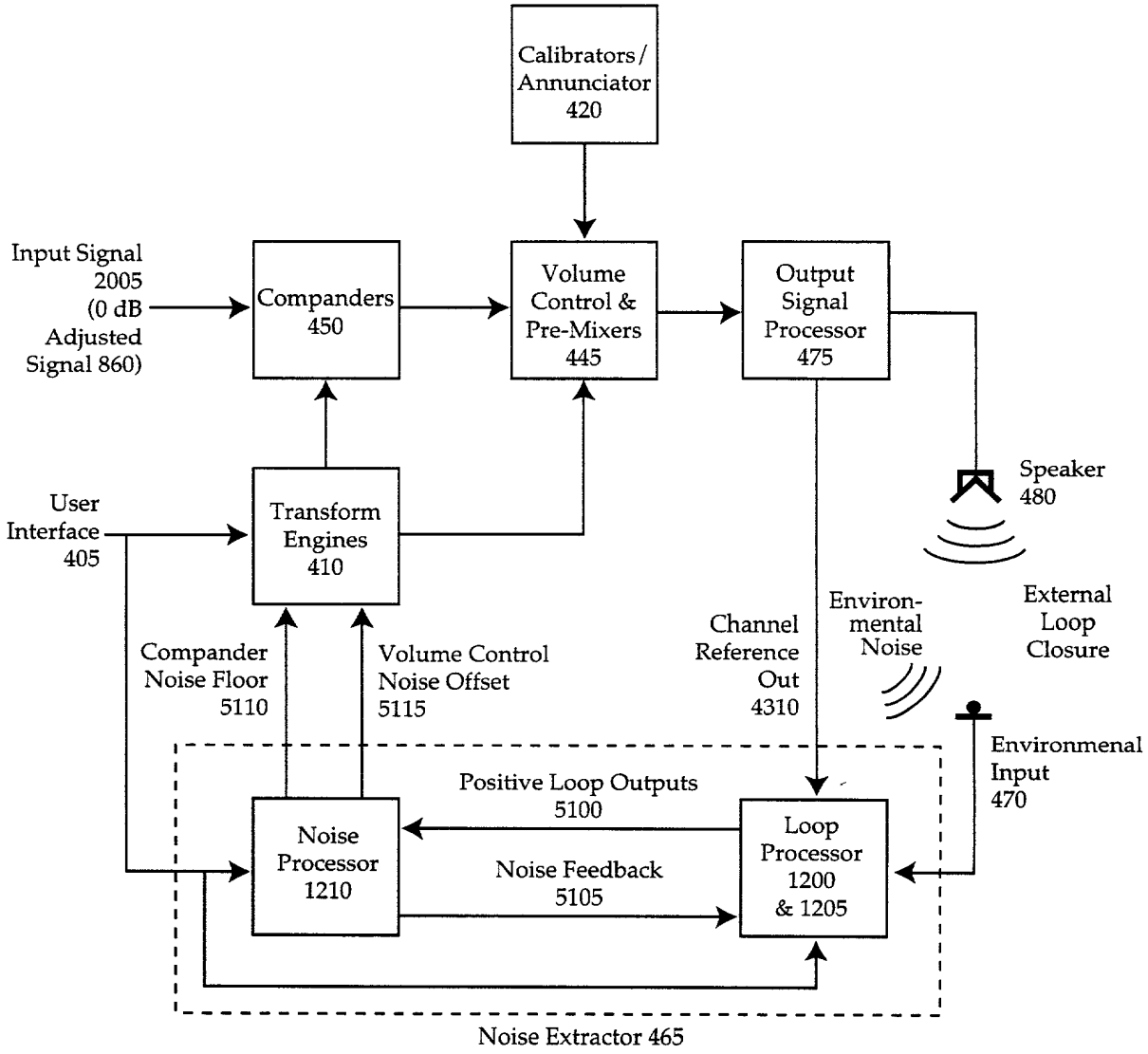

Calibrators / Annunciator 420
Input Signal 2005 (0 dB Adjusted Signal 860)
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Speaker 480
User Interface 405
Transform Engines 410
Compander Noise Floor 5110
Volume Control Noise Offset 5115
Channel Reference Out 4310
Environ-mental Noise
External Loop Closure
Environmenal Input 470
Positive Loop Outputs 5100
Noise Processor 1210
Noise Feedback 5105
Loop Processor 1200 & 1205
Noise Extractor 465

FIG. 51

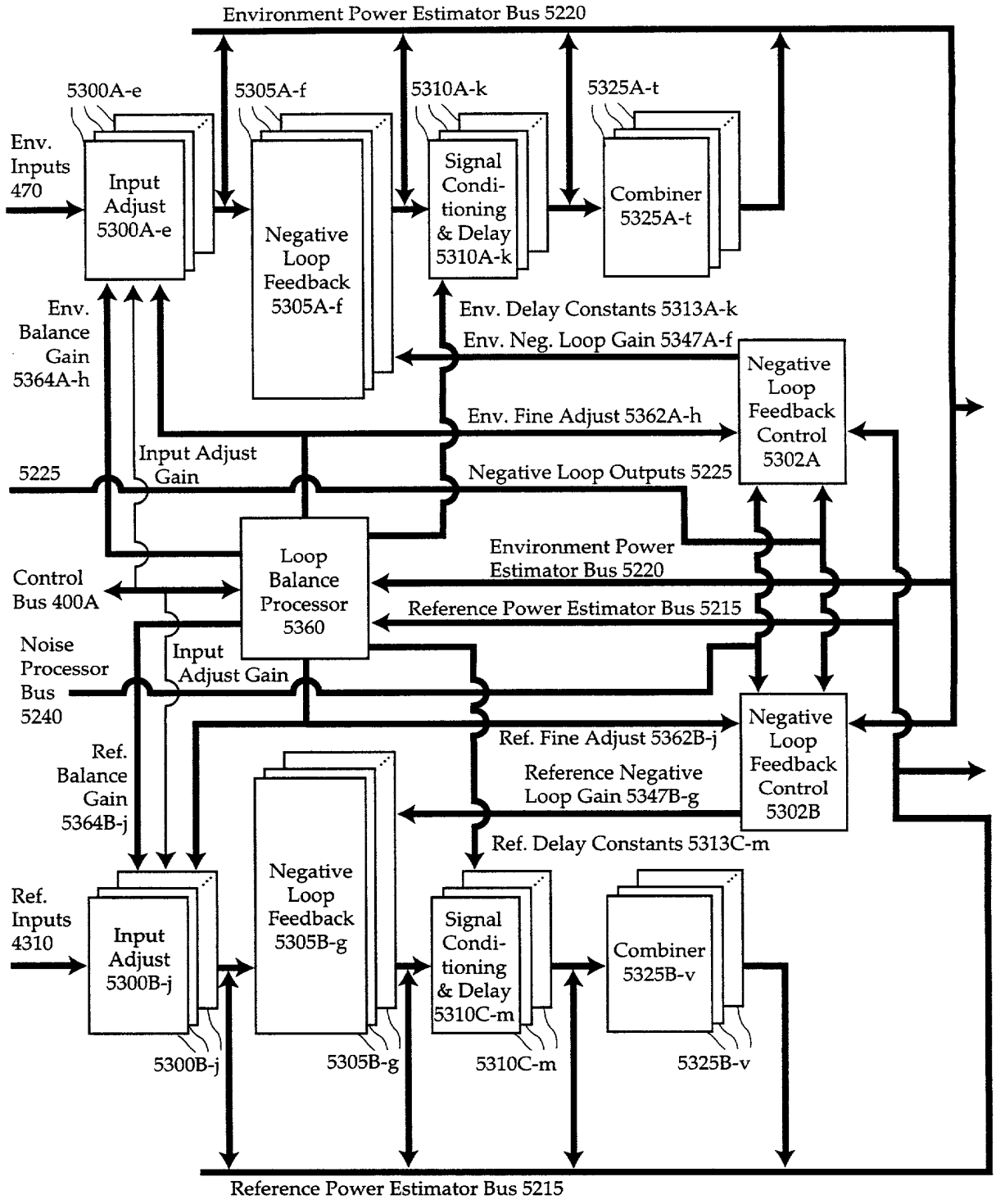

Environment Power Estimator Bus 5220
5300A-e
5305A-f
5310A-k
5325A-t
Env. Inputs 470
Input Adjust 5300A-e
Negative Loop Feedback 5305A-f
Signal Condi-tioning & Delay 5310A-k
Combiner 5325A-t
Env. Balance Gain 5364A-h
Env. Delay Constants 5313A-k
Env. Neg. Loop Gain 5347A-f
Negative Loop Feedback Control 5302A
Env. Fine Adjust 5362A-h
5225
Input Adjust Gain
Negative Loop Outputs 5225
Loop Balance Processor 5360
Environment Power Estimator Bus 5220
Control Bus 400A
Reference Power Estimator Bus 5215
Noise Processor Bus 5240
Input Adjust Gain
Ref. Fine Adjust 5362B-j
Negative Loop Feedback Control 5302B
Ref. Balance Gain 5364B-j
Reference Negative Loop Gain 5347B-g
Ref. Delay Constants 5313C-m
Ref. Inputs 4310
Input Adjust 5300B-j
Negative Loop Feedback 5305B-g
Signal Condi-tioning & Delay 5310C-m
Combiner 5325B-v
5300B-j
5305B-g
5310C-m
5325B-v
Reference Power Estimator Bus 5215

FIG. 52A

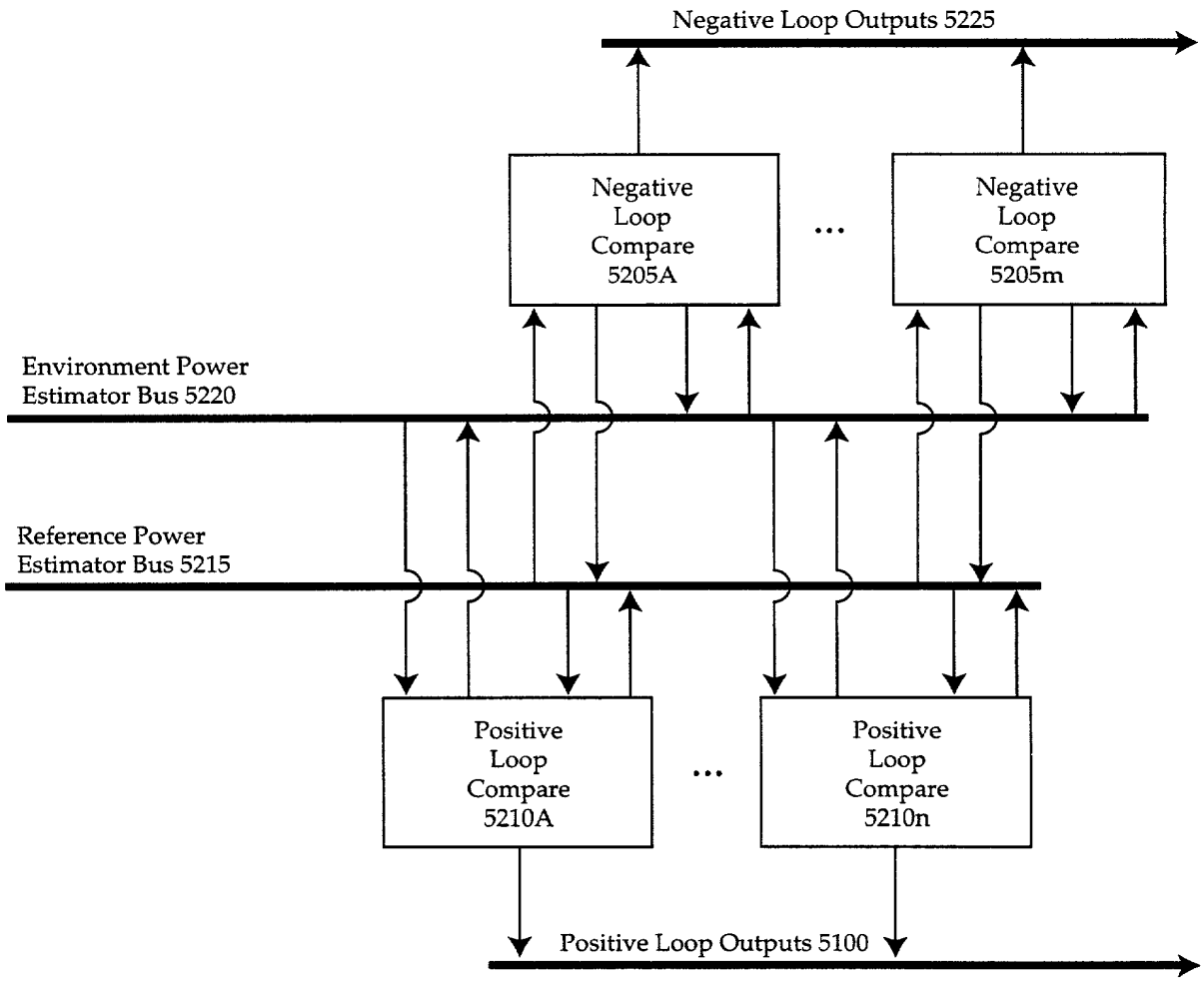

Negative Loop Outputs 5225
Negative Loop Compare 5205A
...
Negative Loop Compare 5205m
Environment Power Estimator Bus 5220
Reference Power Estimator Bus 5215
Positive Loop Compare 5210A
...
Positive Loop Compare 5210n
Positive Loop Outputs 5100

FIG. 52B

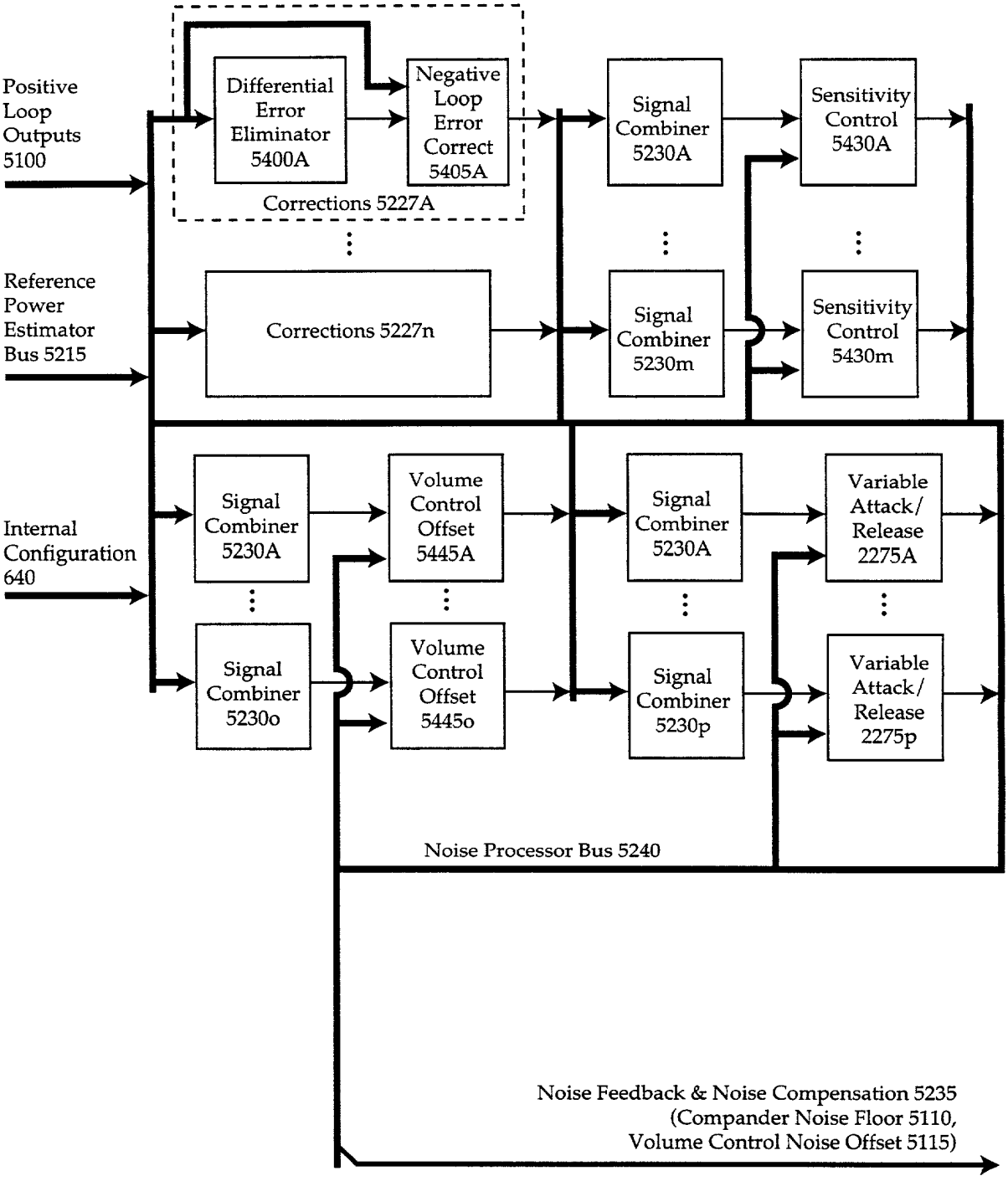

Positive Loop Outputs 5100
Differential Error Eliminator 5400A
Negative Loop Error Correct 5405A
Corrections 5227A
Signal Combiner 5230A
Sensitivity Control 5430A
Reference Power Estimator Bus 5215
Corrections 5227n
Signal Combiner 5230m
Sensitivity Control 5430m
Internal Configuration 640
Signal Combiner 5230A
Volume Control Offset 5445A
Signal Combiner 5230A
Variable Attack/ Release 2275A
Signal Combiner 5230o
Volume Control Offset 5445o
Signal Combiner 5230p
Variable Attack/ Release 2275p
Noise Processor Bus 5240
Noise Feedback & Noise Compensation 5235
(Compander Noise Floor 5110,
Volume Control Noise Offset 5115)

FIG. 52C

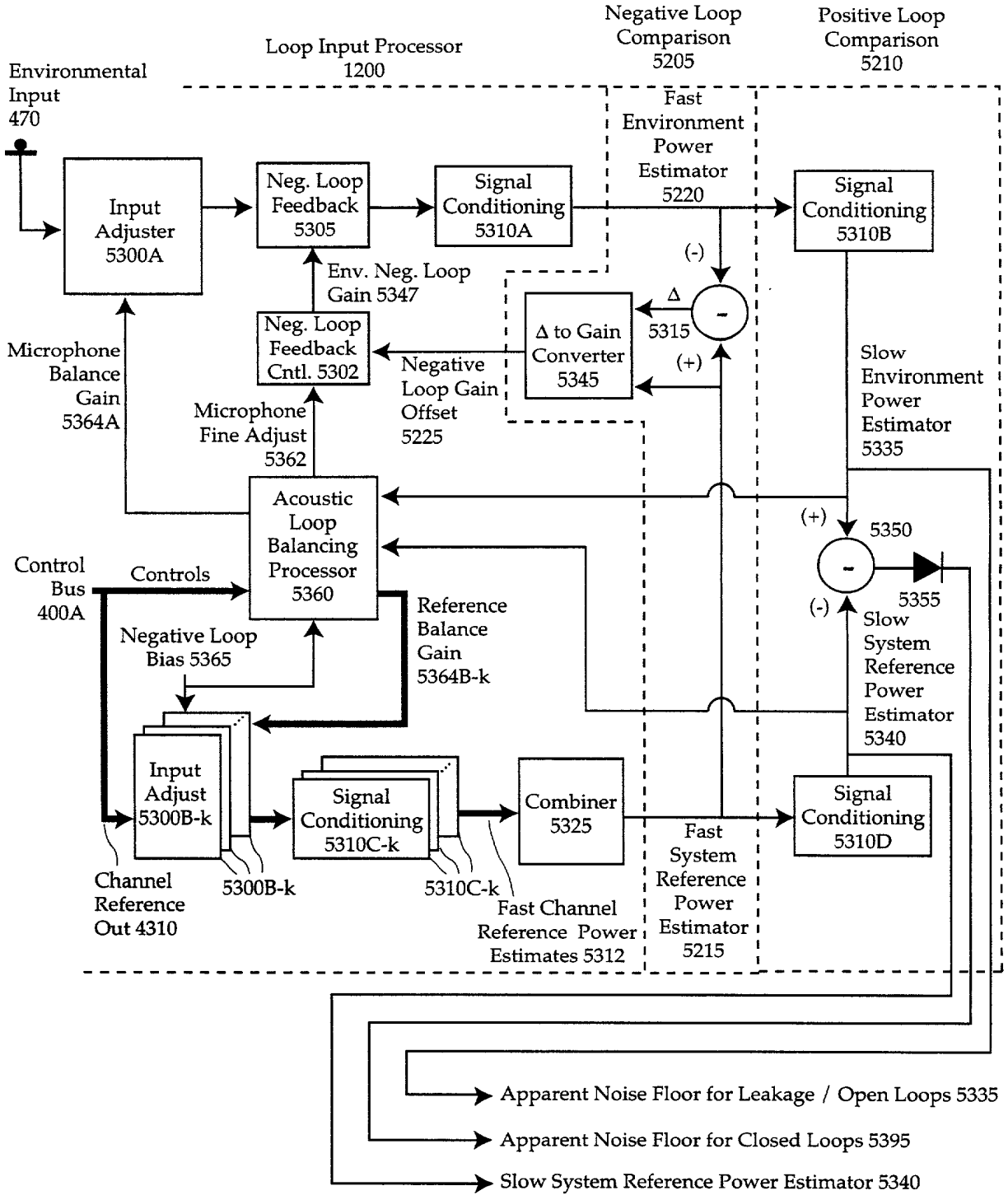

Environmental Input 470
Loop Input Processor 1200
Negative Loop Comparison 5205
Positive Loop Comparison 5210
Input Adjuster 5300A
Neg. Loop Feedback 5305
Signal Conditioning 5310A
Fast Environment Power Estimator 5220
Signal Conditioning 5310B
Env. Neg. Loop Gain 5347
Δ
(-)
5315
(+)
Δ to Gain Converter 5345
Neg. Loop Feedback Cntl. 5302
Negative Loop Gain Offset 5225
Microphone Balance Gain 5364A
Microphone Fine Adjust 5362
Slow Environment Power Estimator 5335
Acoustic Loop Balancing Processor 5360
(+)
5350
(-)
5355
Control Bus 400A
Controls
Negative Loop Bias 5365
Reference Balance Gain 5364B-k
Slow System Reference Power Estimator 5340
Input Adjust 5300B-k
Signal Conditioning 5310C-k
Combiner 5325
Signal Conditioning 5310D
Channel Reference Out 4310
5300B-k
5310C-k
Fast Channel Reference Power Estimates 5312
Fast System Reference Power Estimator 5215
Apparent Noise Floor for Leakage / Open Loops 5335
Apparent Noise Floor for Closed Loops 5395
Slow System Reference Power Estimator 5340

FIG. 53A

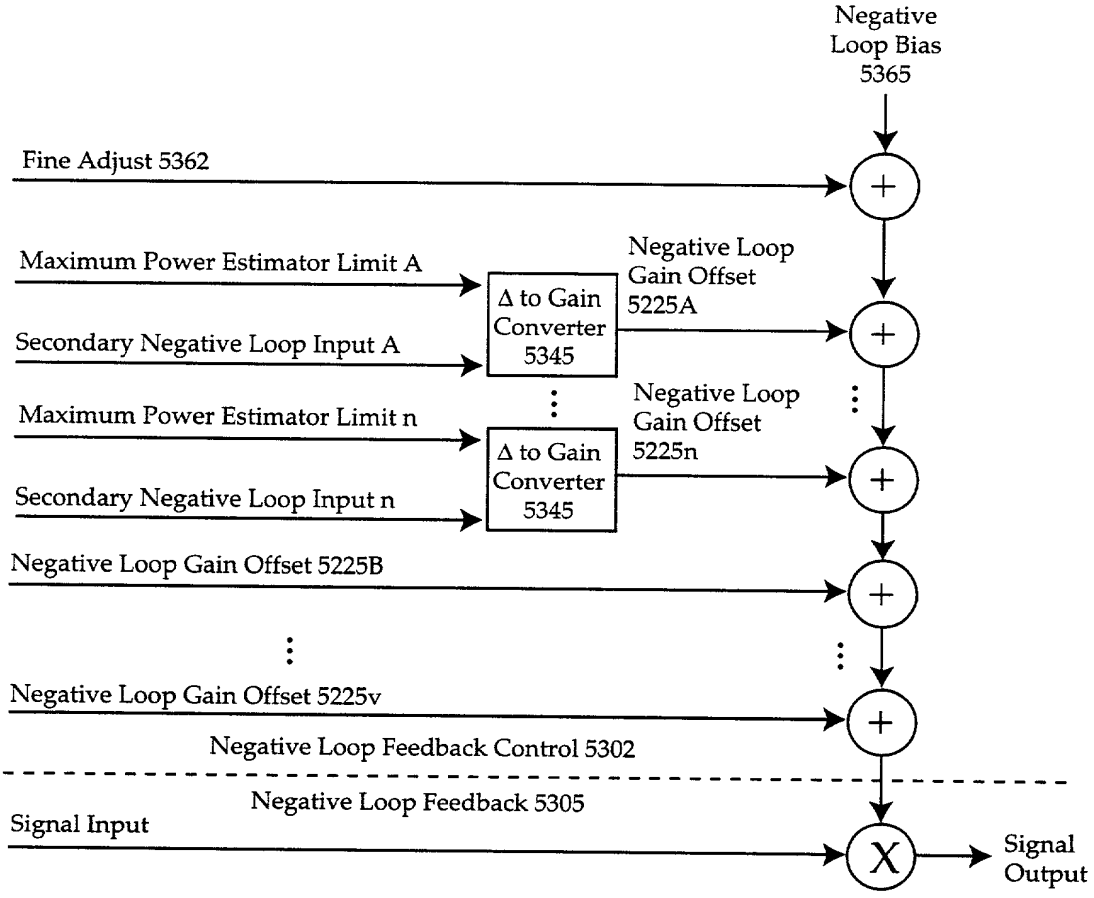

Negative
Loop Bias
5365
Fine Adjust 5362
Maximum Power Estimator Limit A
Secondary Negative Loop Input A
Δ to Gain
Converter
5345
Negative Loop
Gain Offset
5225A
Maximum Power Estimator Limit n
Secondary Negative Loop Input n
Δ to Gain
Converter
5345
Negative Loop
Gain Offset
5225n
Negative Loop Gain Offset 5225B
Negative Loop Gain Offset 5225v
Negative Loop Feedback Control 5302
Negative Loop Feedback 5305
Signal Input
X
Signal
Output

FIG. 53B

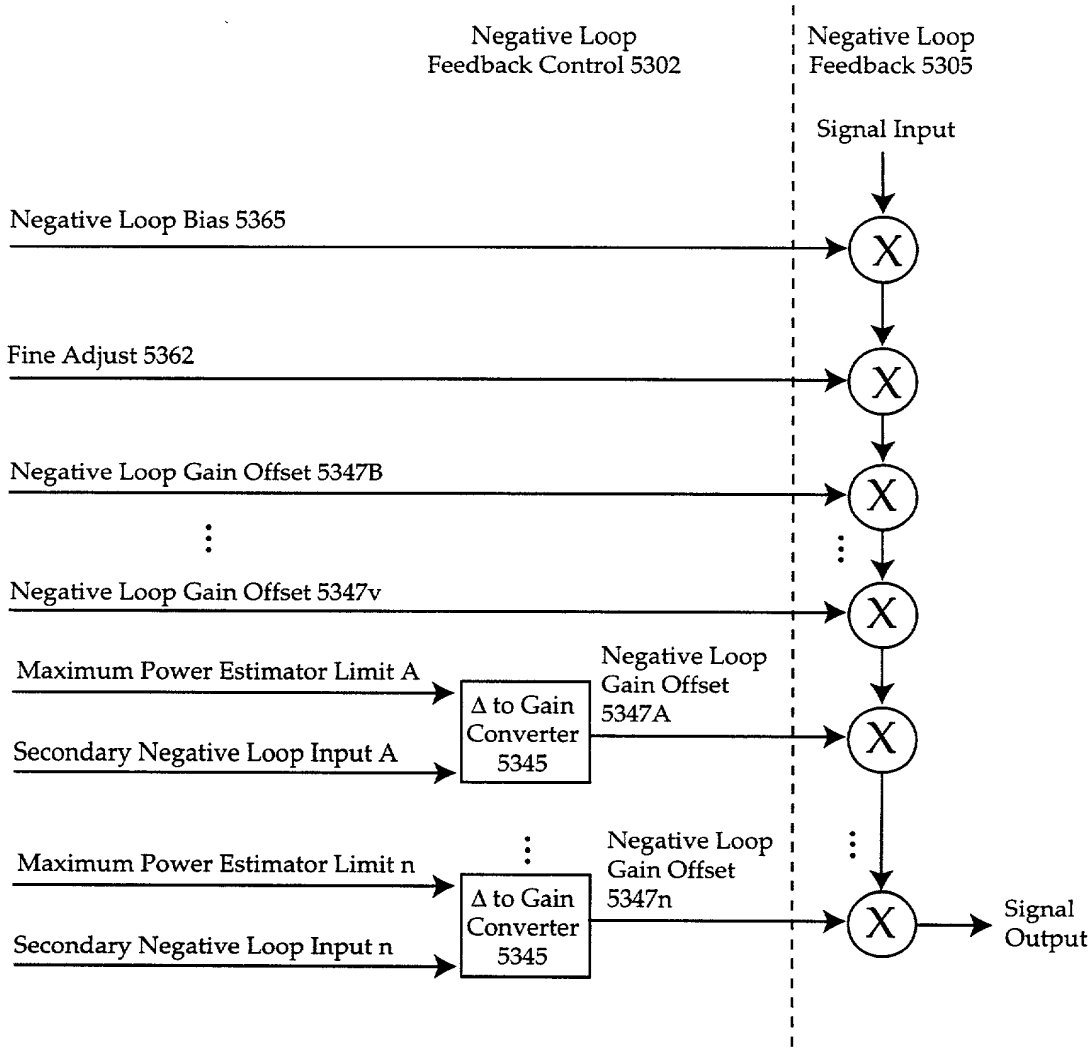

Negative Loop
Feedback Control 5302
Negative Loop
Feedback 5305
Signal Input
Negative Loop Bias 5365
Fine Adjust 5362
Negative Loop Gain Offset 5347B
Negative Loop Gain Offset 5347v
Maximum Power Estimator Limit A
Secondary Negative Loop Input A
Δ to Gain
Converter
5345
Negative Loop
Gain Offset
5347A
Maximum Power Estimator Limit n
Secondary Negative Loop Input n
Δ to Gain
Converter
5345
Negative Loop
Gain Offset
5347n
X
Signal
Output

FIG. 53C

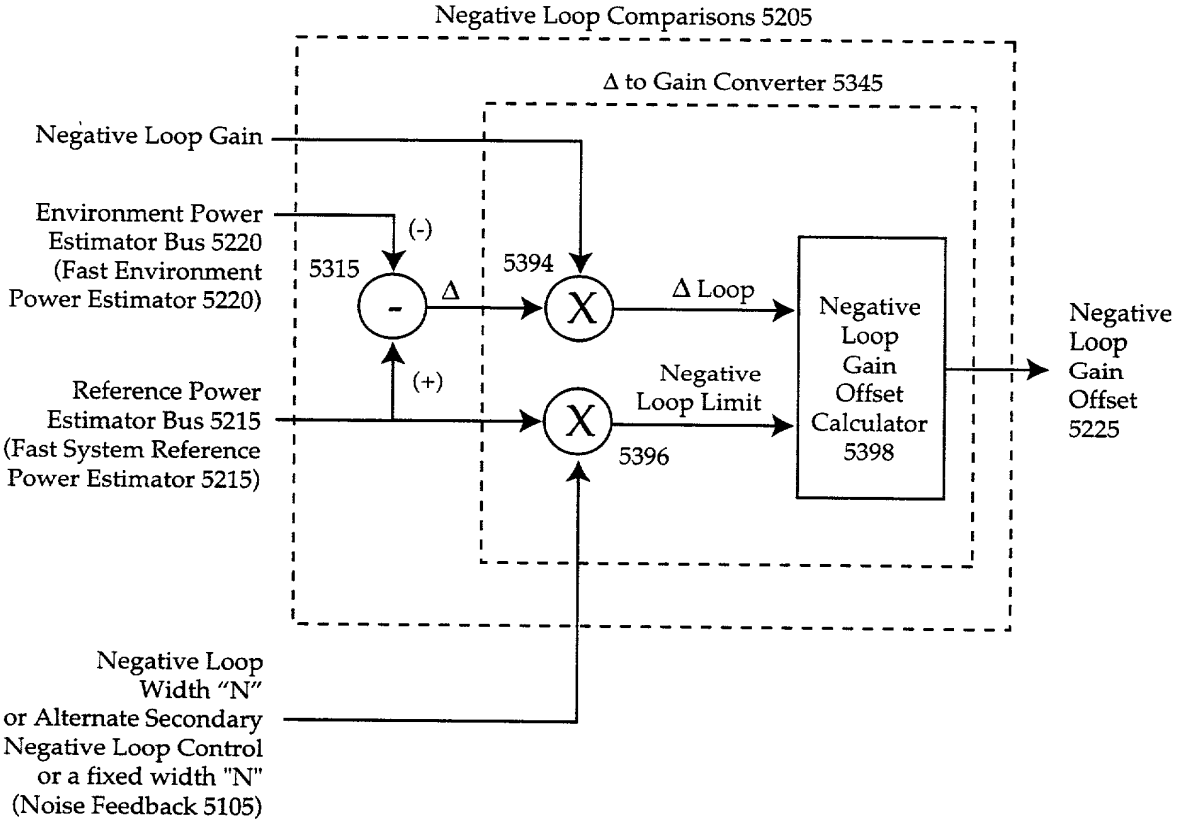

Negative Loop Comparisons 5205
Δ to Gain Converter 5345
Negative Loop Gain
Environment Power Estimator Bus 5220 (Fast Environment Power Estimator 5220)
(-)
5315
-
Δ
5394
X
Δ Loop
Negative Loop Gain Offset Calculator 5398
Negative Loop Gain Offset 5225
(+)
Reference Power Estimator Bus 5215 (Fast System Reference Power Estimator 5215)
X
Negative Loop Limit
5396
Negative Loop Width "N" or Alternate Secondary Negative Loop Control or a fixed width "N" (Noise Feedback 5105)

FIG. 53D

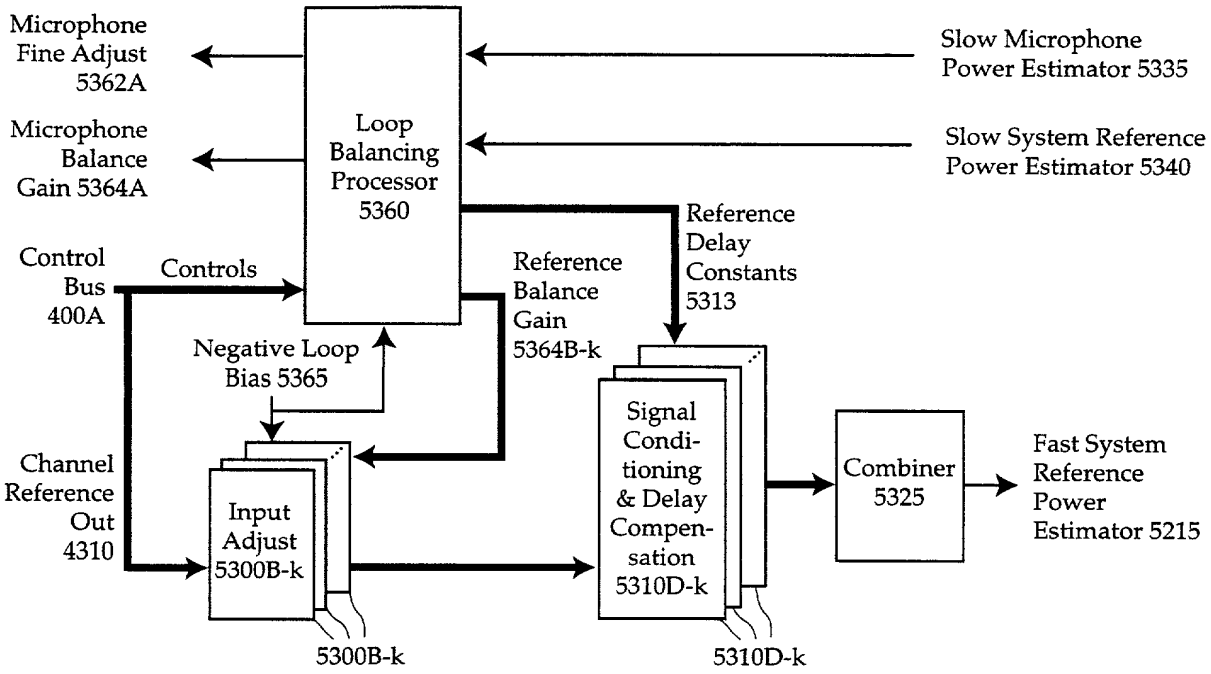


FIG. 53E

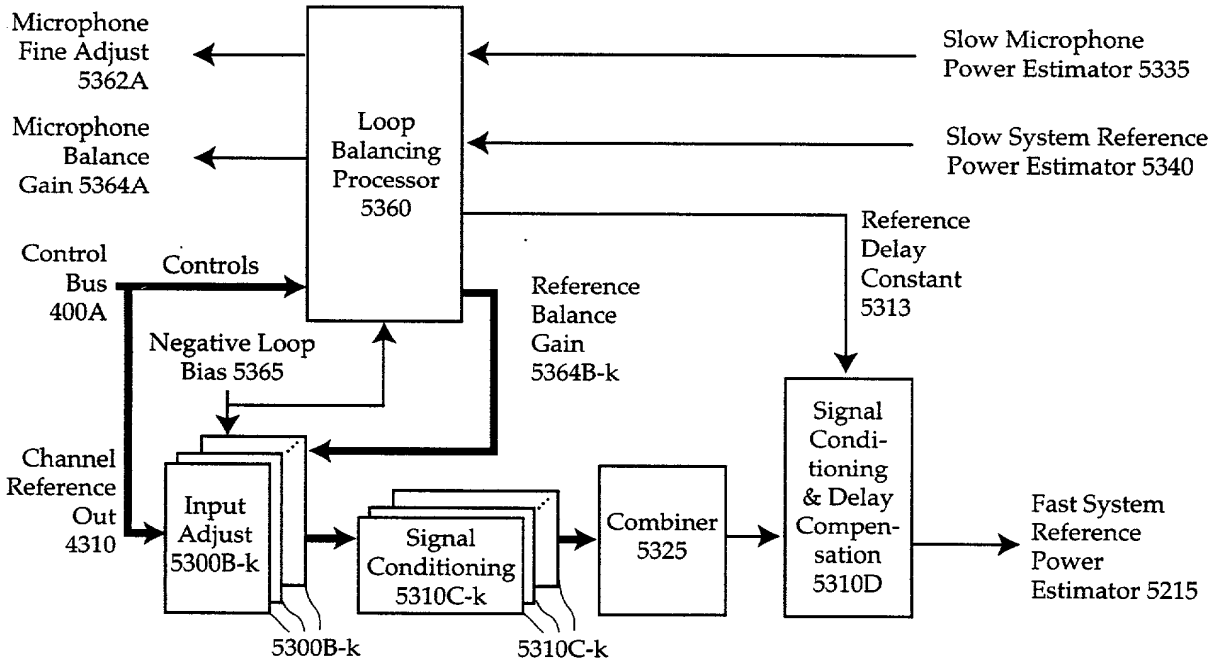


FIG. 53F

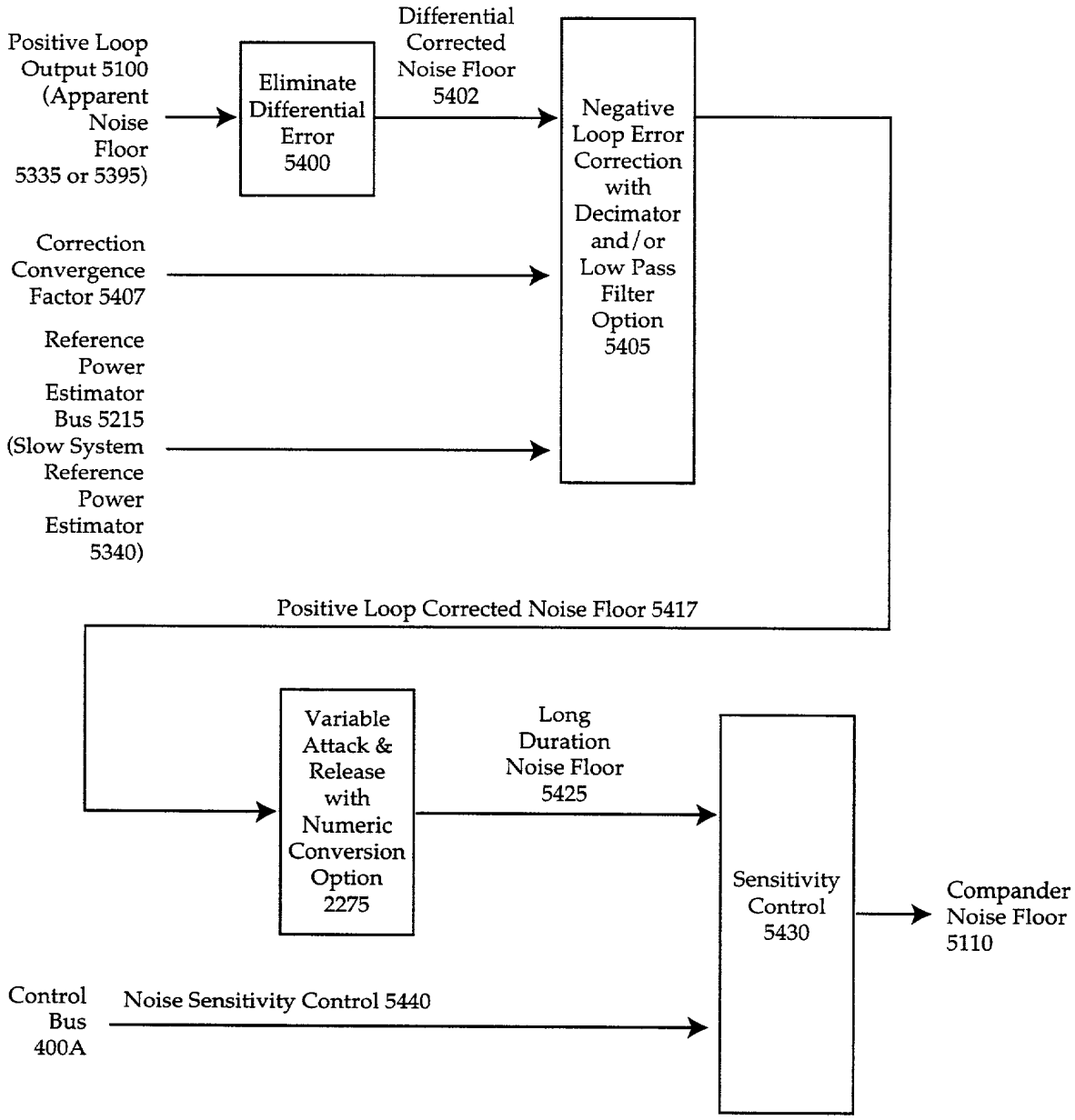

Positive Loop Output 5100 (Apparent Noise Floor 5335 or 5395)
Eliminate Differential Error 5400
Differential Corrected Noise Floor 5402
Negative Loop Error Correction with Decimator and/or Low Pass Filter Option 5405
Correction Convergence Factor 5407
Reference Power Estimator Bus 5215 (Slow System Reference Power Estimator 5340)
Positive Loop Corrected Noise Floor 5417
Variable Attack & Release with Numeric Conversion Option 2275
Long Duration Noise Floor 5425
Sensitivity Control 5430
Compander Noise Floor 5110
Control Bus 400A
Noise Sensitivity Control 5440

FIG. 54A

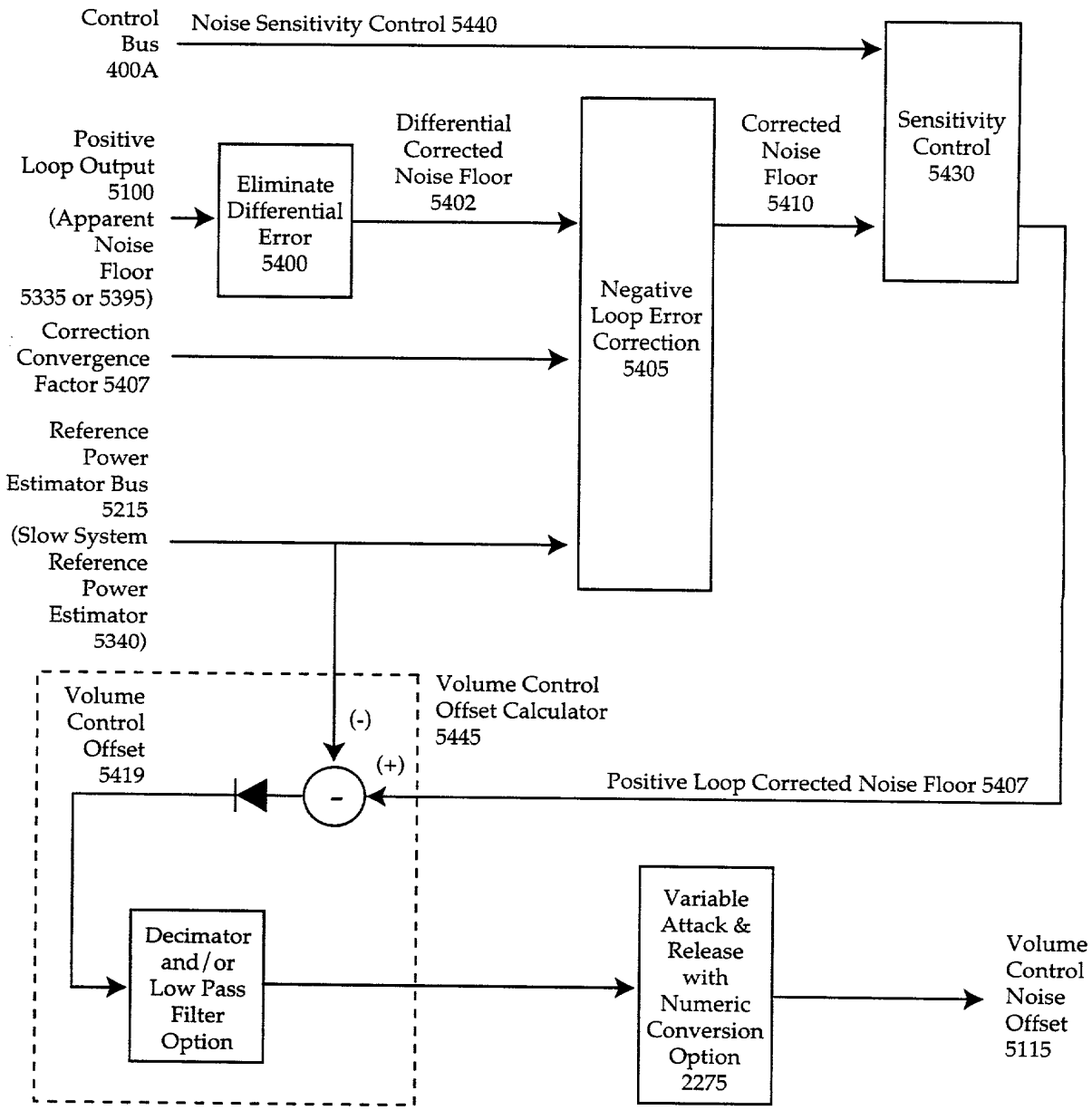

Control Bus 400A
Noise Sensitivity Control 5440
Positive Loop Output 5100 (Apparent Noise Floor 5335 or 5395)
Eliminate Differential Error 5400
Differential Corrected Noise Floor 5402
Negative Loop Error Correction 5405
Corrected Noise Floor 5410
Sensitivity Control 5430
Correction Convergence Factor 5407
Reference Power Estimator Bus 5215 (Slow System Reference Power Estimator 5340)
Volume Control Offset 5419
Volume Control Offset Calculator 5445
(-)
(+)
Positive Loop Corrected Noise Floor 5407
Decimator and/or Low Pass Filter Option
Variable Attack & Release with Numeric Conversion Option 2275
Volume Control Noise Offset 5115

FIG. 54B

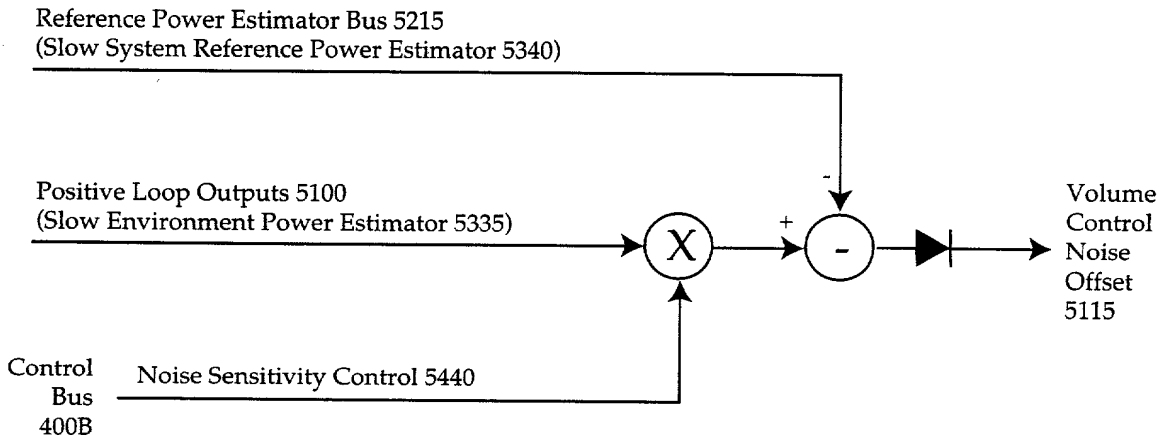


FIG. 54C

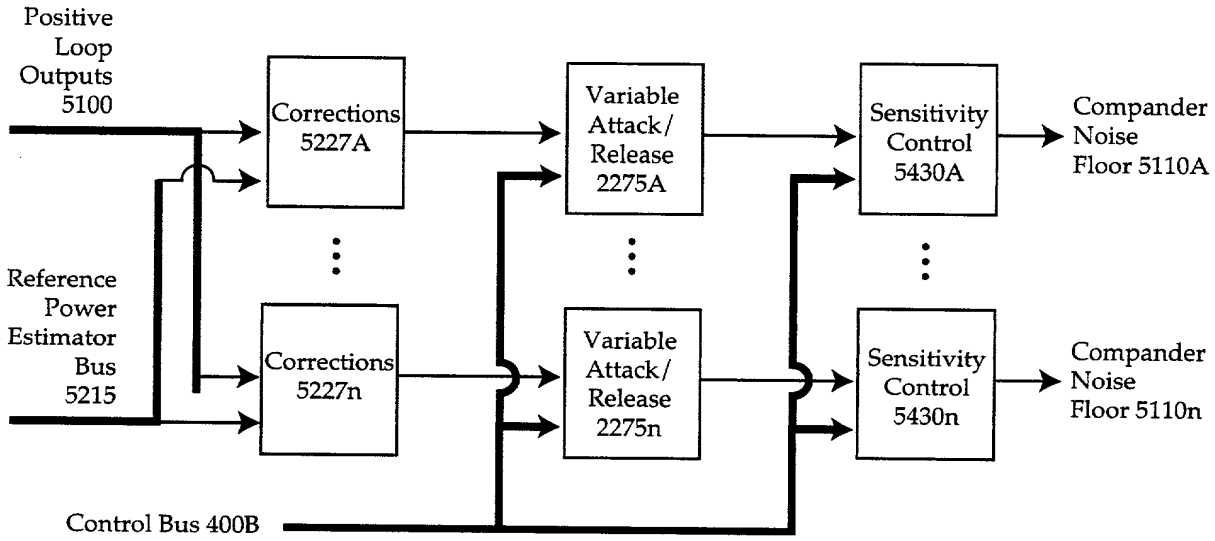


FIG. 54D

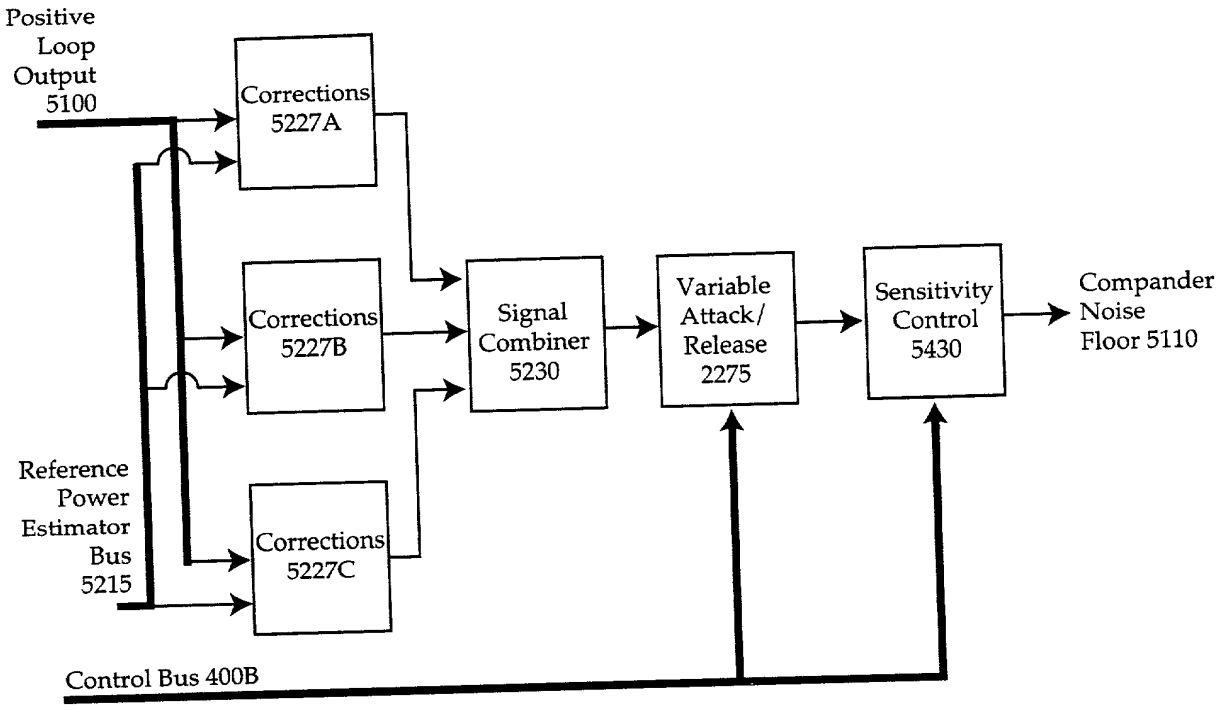


FIG. 54E

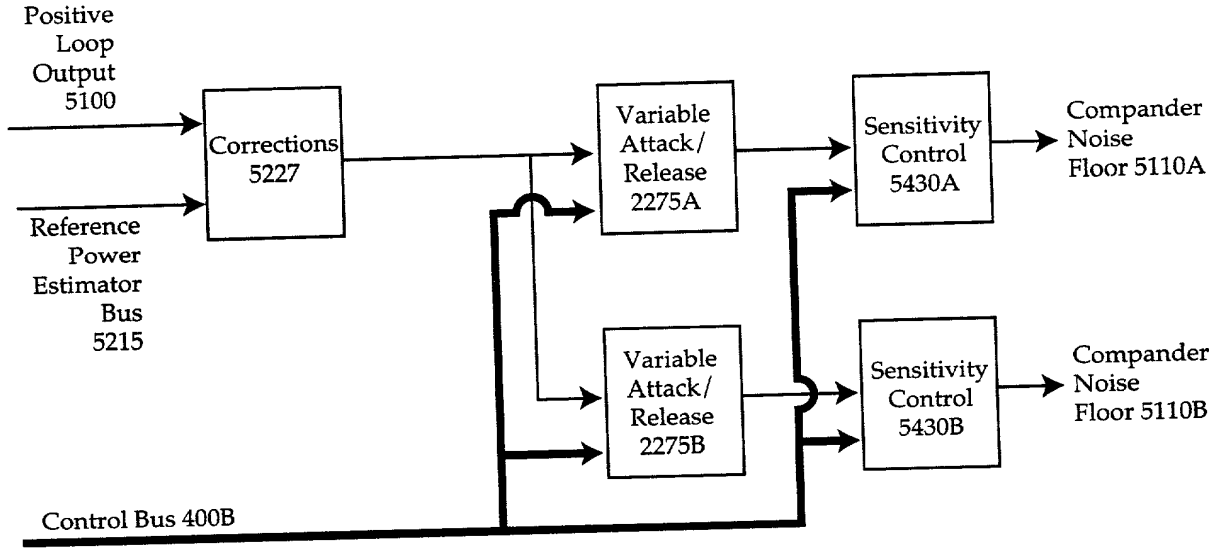


FIG. 54F

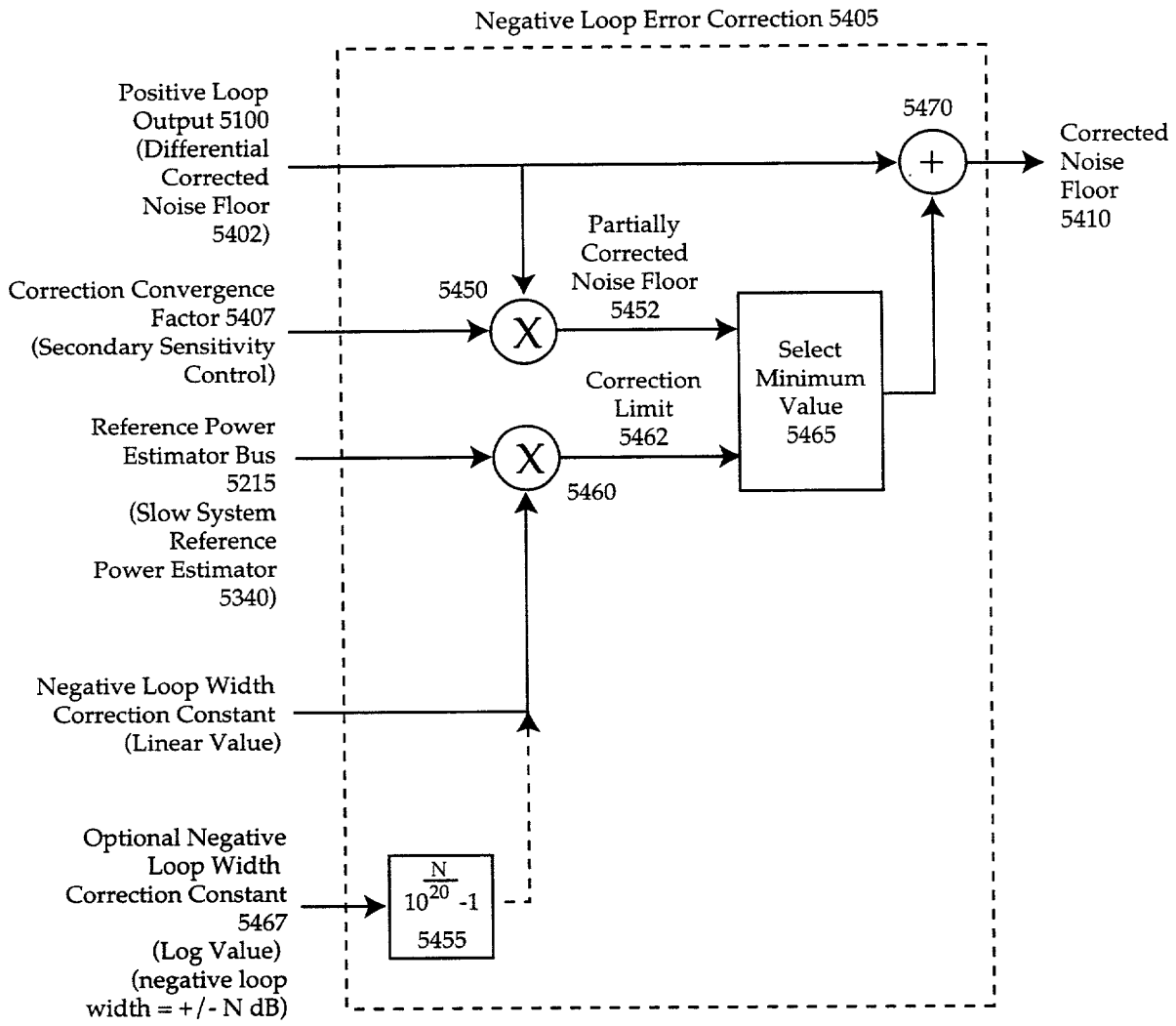

Negative Loop Error Correction 5405
Positive Loop Output 5100 (Differential Corrected Noise Floor 5402)
Correction Convergence Factor 5407 (Secondary Sensitivity Control)
Reference Power Estimator Bus 5215 (Slow System Reference Power Estimator 5340)
Negative Loop Width Correction Constant (Linear Value)
Optional Negative Loop Width Correction Constant 5467 (Log Value) (negative loop width = +/- N dB)
5450
X
Partially Corrected Noise Floor 5452
Correction Limit 5462
X
5460
Select Minimum Value 5465
5470
+
Corrected Noise Floor 5410
N/20
10 -1
5455

FIG. 54G

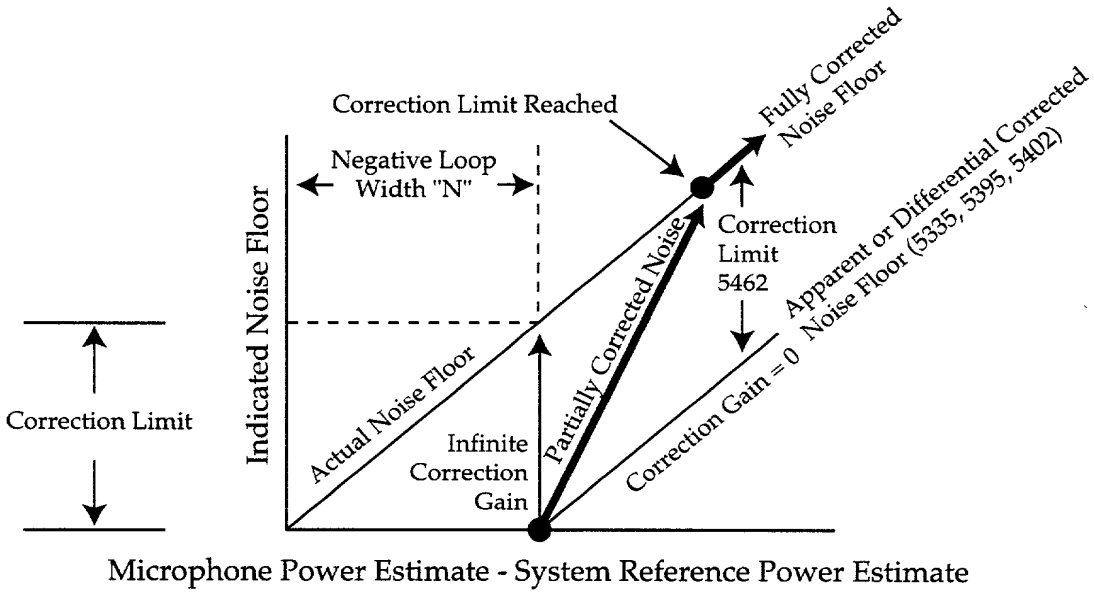

Correction Limit Reached
Fully Corrected Noise Floor
Negative Loop Width "N"
Indicated Noise Floor
Correction Limit 5462
Apparent or Differential Corrected Noise Floor (5335, 5395, 5402)
Partially Corrected Noise
Actual Noise Floor
Correction Limit
Infinite Correction Gain
Correction Gain = 0
Microphone Power Estimate - System Reference Power Estimate

FIG. 54H

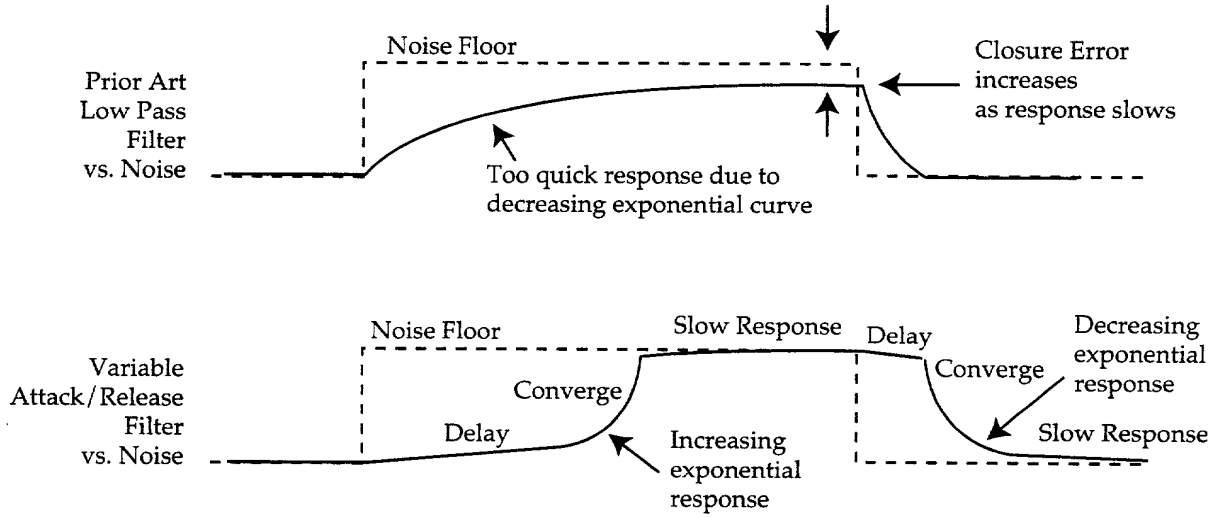


FIG. 55A

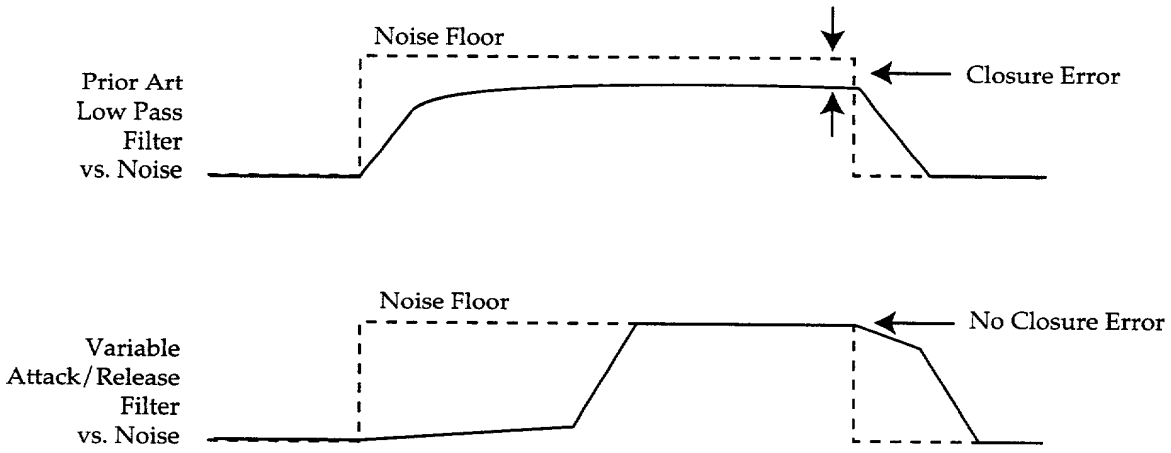


FIG. 55B

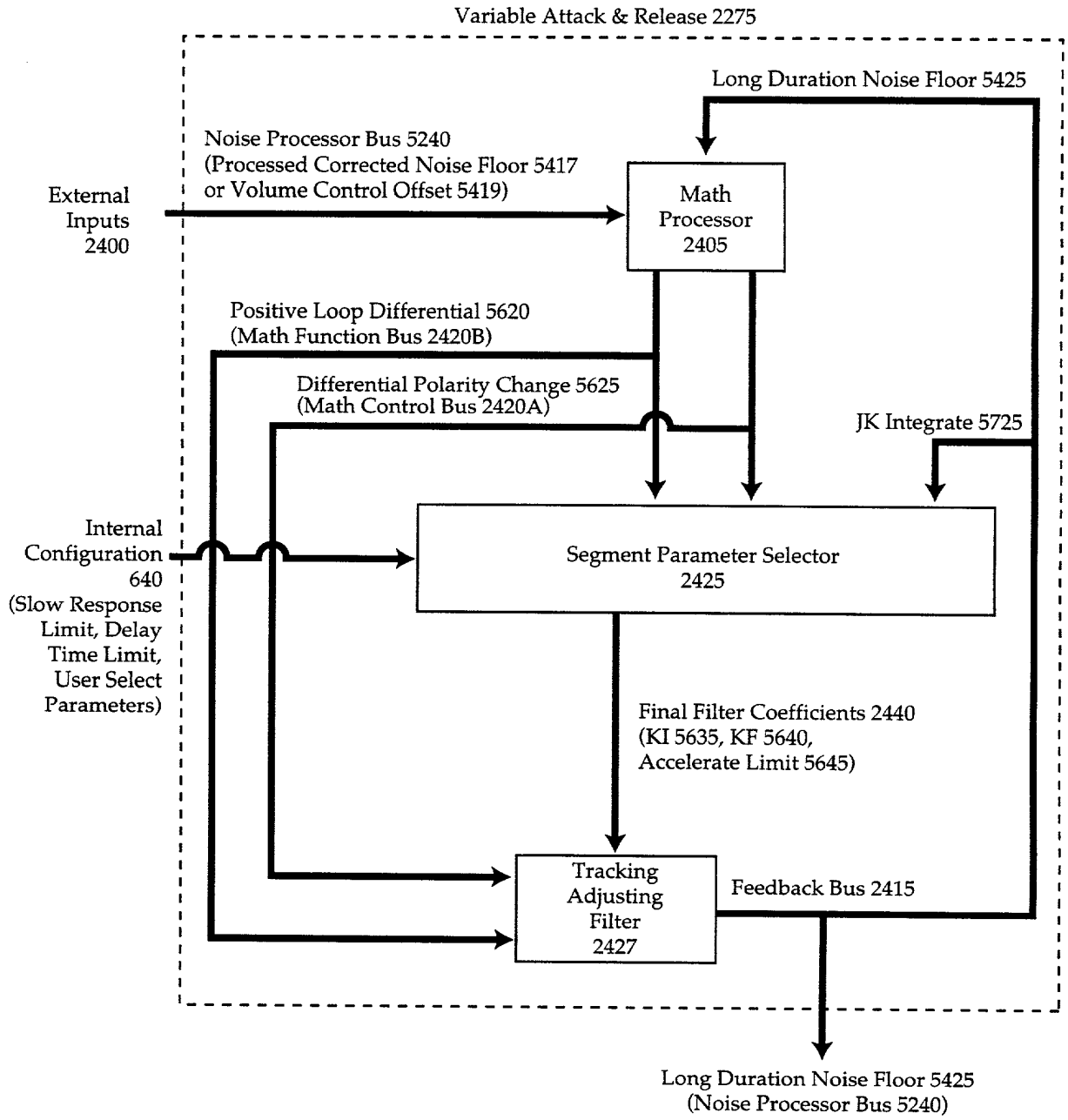

Variable Attack & Release 2275
Long Duration Noise Floor 5425
Noise Processor Bus 5240
(Processed Corrected Noise Floor 5417
or Volume Control Offset 5419)
External
Inputs
2400
Math
Processor
2405
Positive Loop Differential 5620
(Math Function Bus 2420B)
Differential Polarity Change 5625
(Math Control Bus 2420A)
JK Integrate 5725
Internal
Configuration
640
(Slow Response
Limit, Delay
Time Limit,
User Select
Parameters)
Segment Parameter Selector
2425
Final Filter Coefficients 2440
(KI 5635, KF 5640,
Accelerate Limit 5645)
Tracking
Adjusting
Filter
2427
Feedback Bus 2415
Long Duration Noise Floor 5425
(Noise Processor Bus 5240)

FIG. 55C

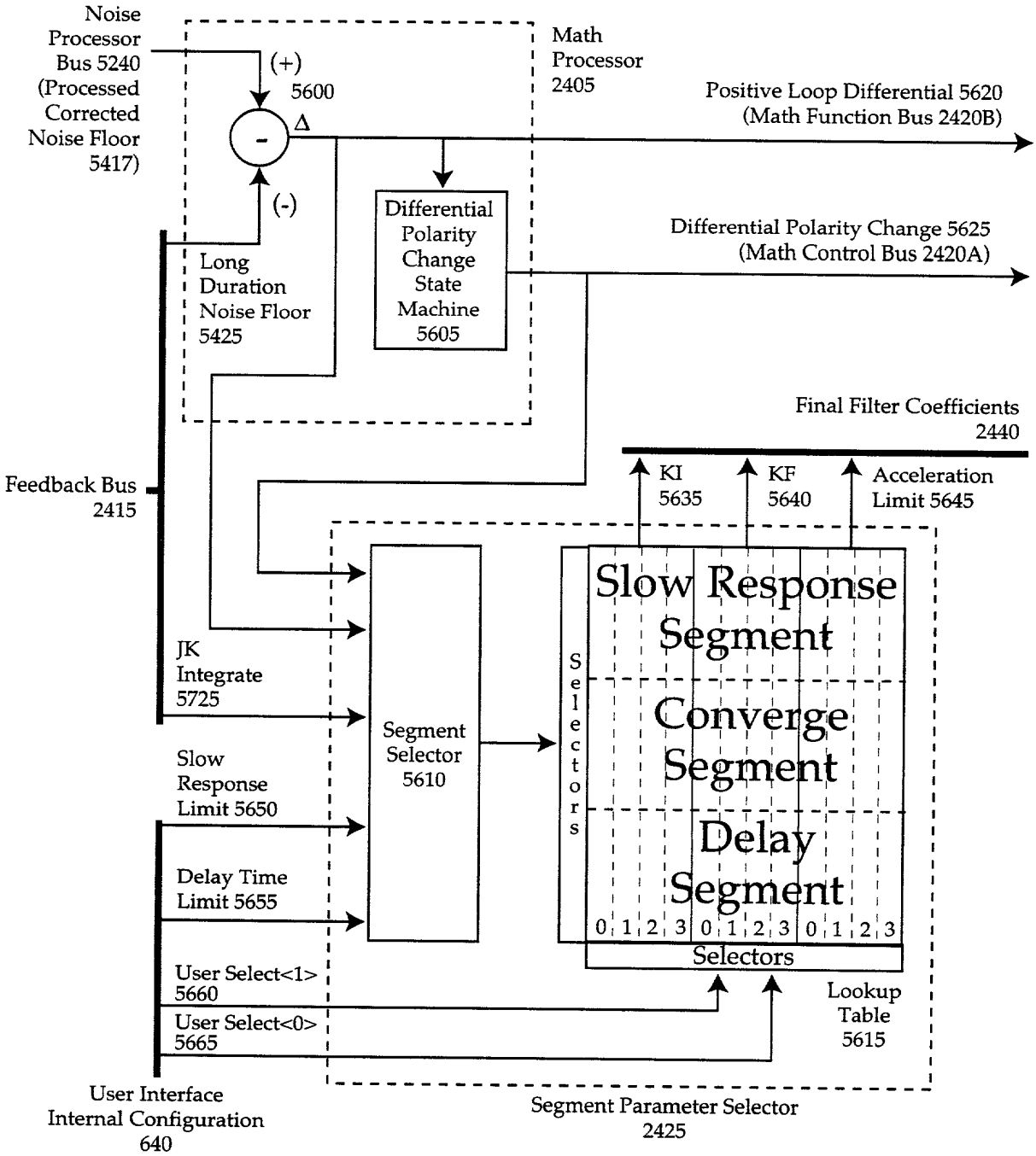

Noise Processor Bus 5240 (Processed Corrected Noise Floor 5417)
(+)
5600
Δ
(-)
Long Duration Noise Floor 5425
Differential Polarity Change State Machine 5605
Math Processor 2405
Positive Loop Differential 5620 (Math Function Bus 2420B)
Differential Polarity Change 5625 (Math Control Bus 2420A)
Final Filter Coefficients 2440
KI 5635
KF 5640
Acceleration Limit 5645
Feedback Bus 2415
JK Integrate 5725
Slow Response Limit 5650
Delay Time Limit 5655
Segment Selector 5610
Slow Response Segment
Converge Segment
Delay Segment
Selectors
0 1 2 3 0 1 2 3 0 1 2 3
Selectors
User Select<1> 5660
User Select<0> 5665
Lookup Table 5615
User Interface Internal Configuration 640
Segment Parameter Selector 2425

FIG. 56

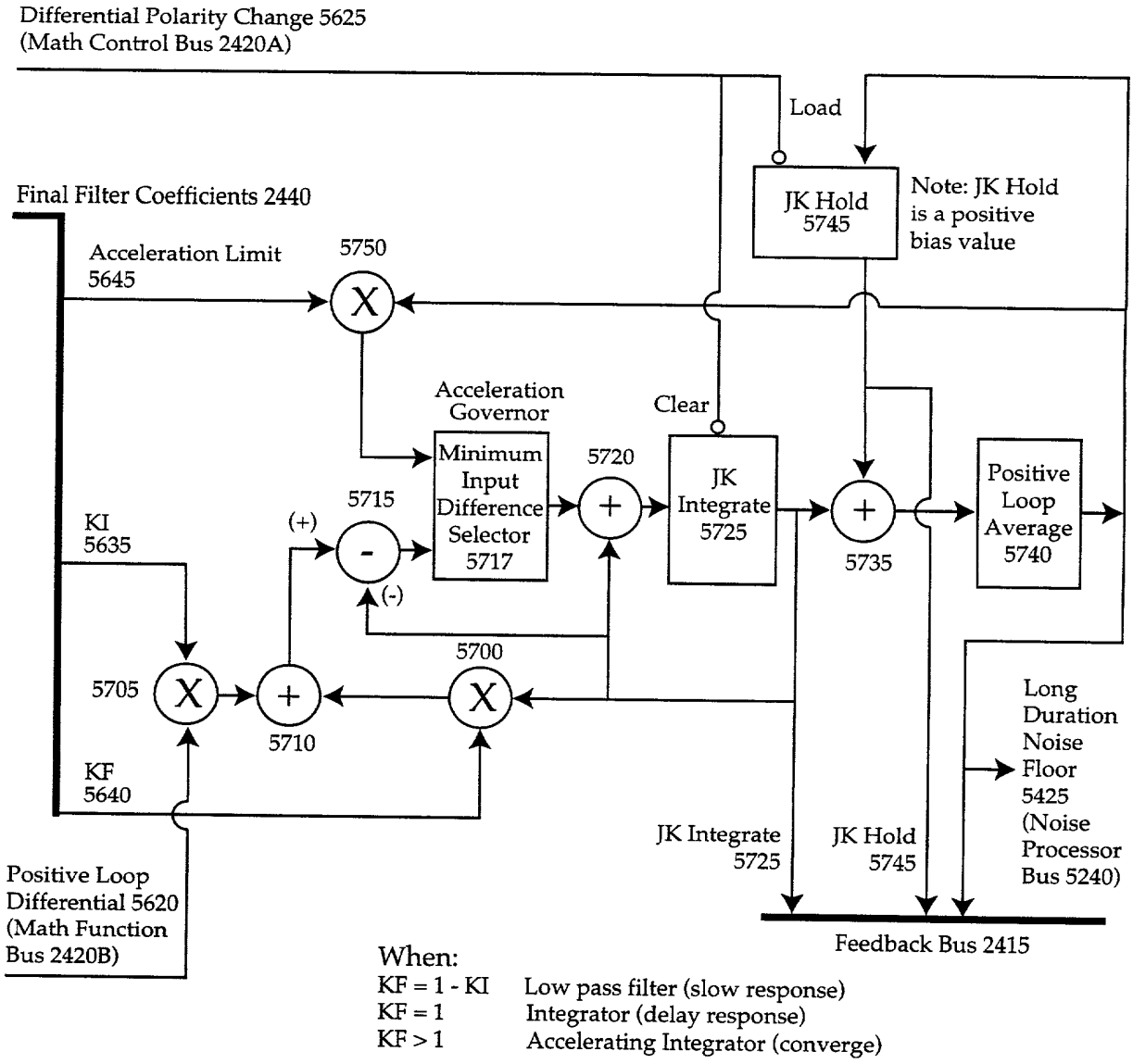

Differential Polarity Change 5625
(Math Control Bus 2420A)
Load
JK Hold
5745
Note: JK Hold
is a positive
bias value
Final Filter Coefficients 2440
Acceleration Limit
5645
5750
Acceleration
Governor
Clear
Minimum
Input
Difference
Selector
5717
5720
JK
Integrate
5725
Positive
Loop
Average
5740
5735
KI
5635
5715
(+)
(-)
5700
5705
5710
KF
5640
Long
Duration
Noise
Floor
5425
(Noise
Processor
Bus 5240)
JK Integrate
5725
JK Hold
5745
Feedback Bus 2415
Positive Loop
Differential 5620
(Math Function
Bus 2420B)
When:
KF = 1 - KI Low pass filter (slow response)
KF = 1 Integrator (delay response)
KF > 1 Accelerating Integrator (converge)

FIG. 57A

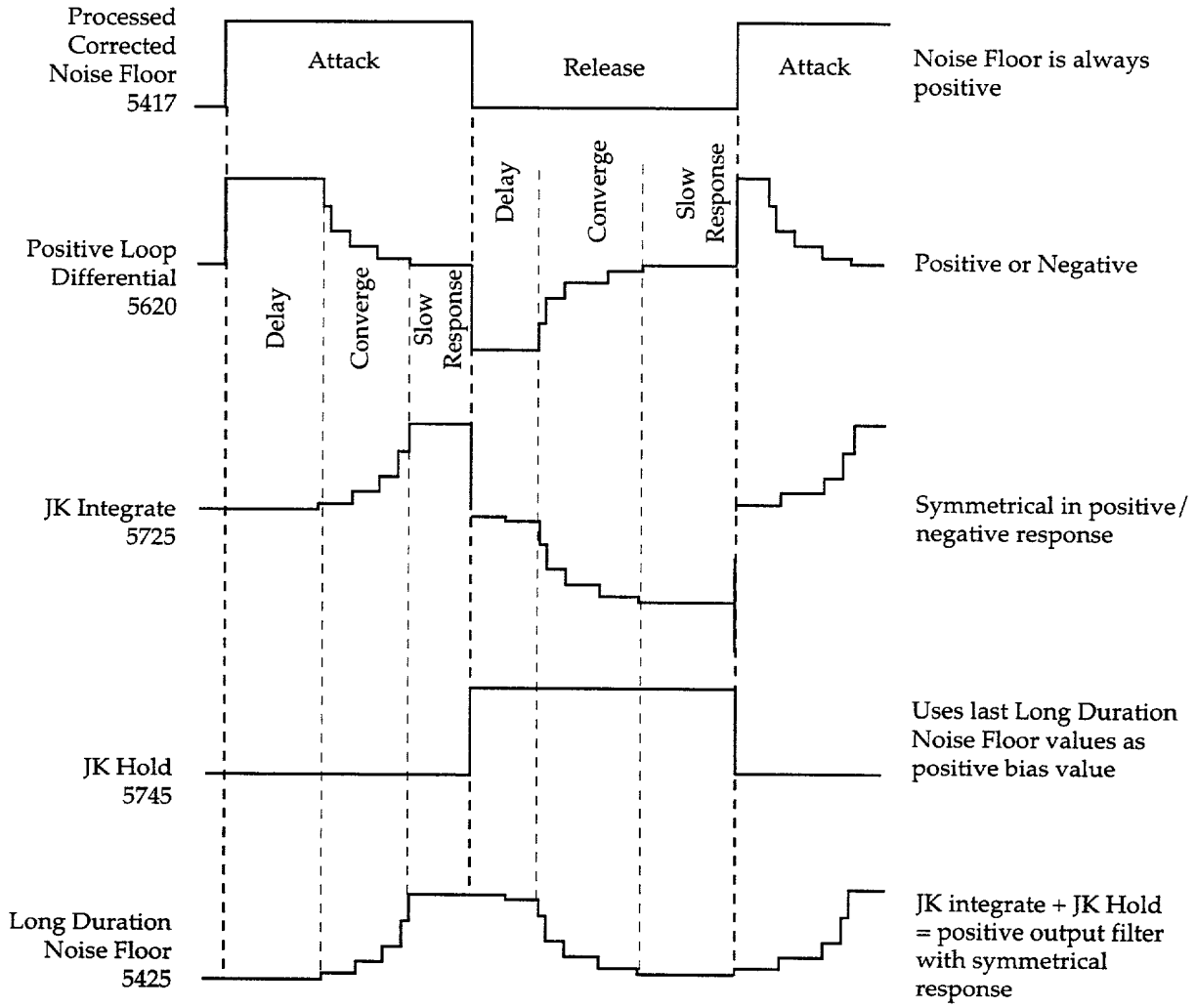

Processed Corrected Noise Floor 5417
Attack
Release
Attack
Noise Floor is always positive
Positive Loop Differential 5620
Delay
Converge
Slow Response
Delay
Converge
Slow Response
Positive or Negative
JK Integrate 5725
Symmetrical in positive/ negative response
JK Hold 5745
Uses last Long Duration Noise Floor values as positive bias value
Long Duration Noise Floor 5425
JK integrate + JK Hold = positive output filter with symmetrical response

FIG. 57B

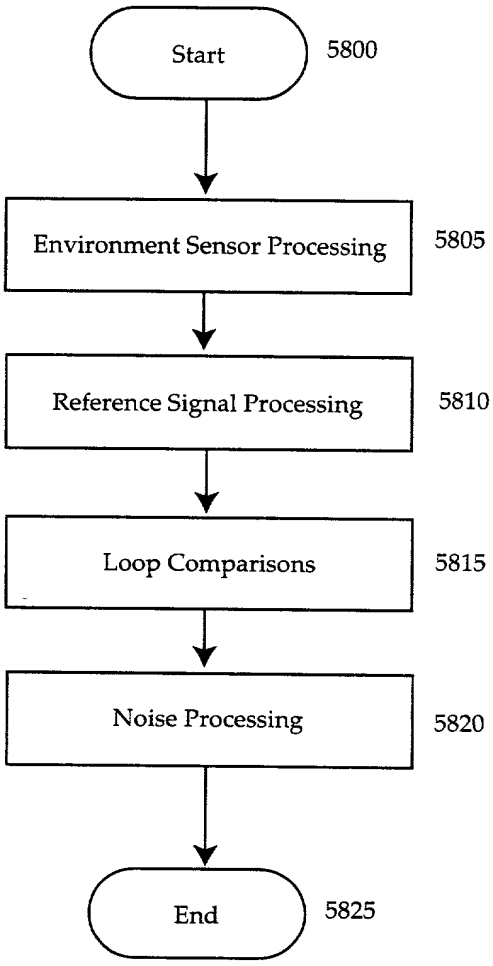

Start
5800
Environment Sensor Processing
5805
Reference Signal Processing
5810
Loop Comparisons
5815
Noise Processing
5820
End
5825

FIG. 58

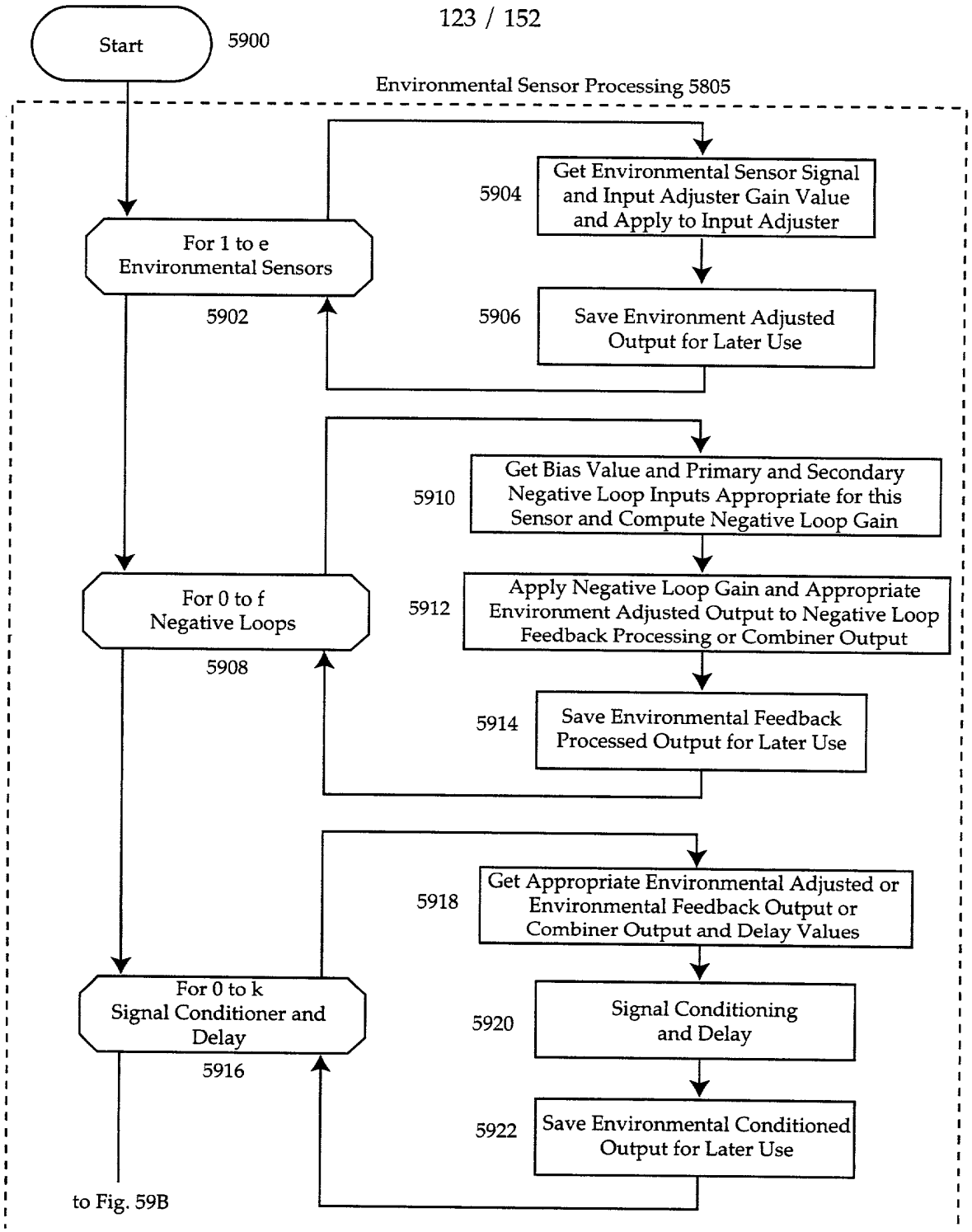

Start
5900
Environmental Sensor Processing 5805
For 1 to e
Environmental Sensors
5902
5904
Get Environmental Sensor Signal and Input Adjuster Gain Value and Apply to Input Adjuster
5906
Save Environment Adjusted Output for Later Use
For 0 to f
Negative Loops
5908
5910
Get Bias Value and Primary and Secondary Negative Loop Inputs Appropriate for this Sensor and Compute Negative Loop Gain
5912
Apply Negative Loop Gain and Appropriate Environment Adjusted Output to Negative Loop Feedback Processing or Combiner Output
5914
Save Environmental Feedback Processed Output for Later Use
For 0 to k
Signal Conditioner and Delay
5916
5918
Get Appropriate Environmental Adjusted or Environmental Feedback Output or Combiner Output and Delay Values
5920
Signal Conditioning and Delay
5922
Save Environmental Conditioned Output for Later Use
to Fig. 59B

FIG. 59A

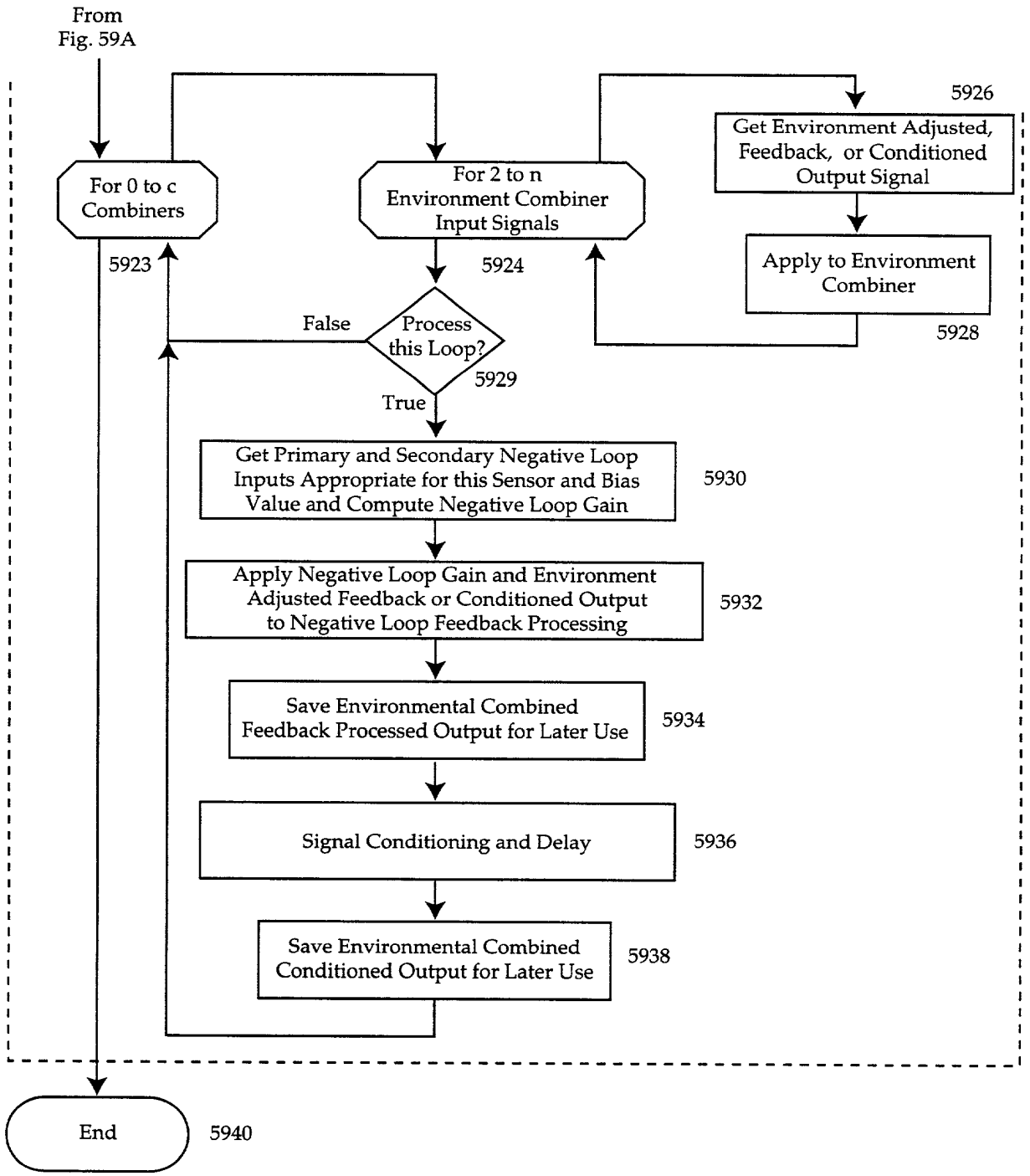

From Fig. 59A
For 0 to c Combiners
5923
For 2 to n Environment Combiner Input Signals
5924
5926
Get Environment Adjusted, Feedback, or Conditioned Output Signal
Apply to Environment Combiner
5928
False
Process this Loop?
5929
True
Get Primary and Secondary Negative Loop Inputs Appropriate for this Sensor and Bias Value and Compute Negative Loop Gain
5930
Apply Negative Loop Gain and Environment Adjusted Feedback or Conditioned Output to Negative Loop Feedback Processing
5932
Save Environmental Combined Feedback Processed Output for Later Use
5934
Signal Conditioning and Delay
5936
Save Environmental Combined Conditioned Output for Later Use
5938
End
5940

FIG. 59B

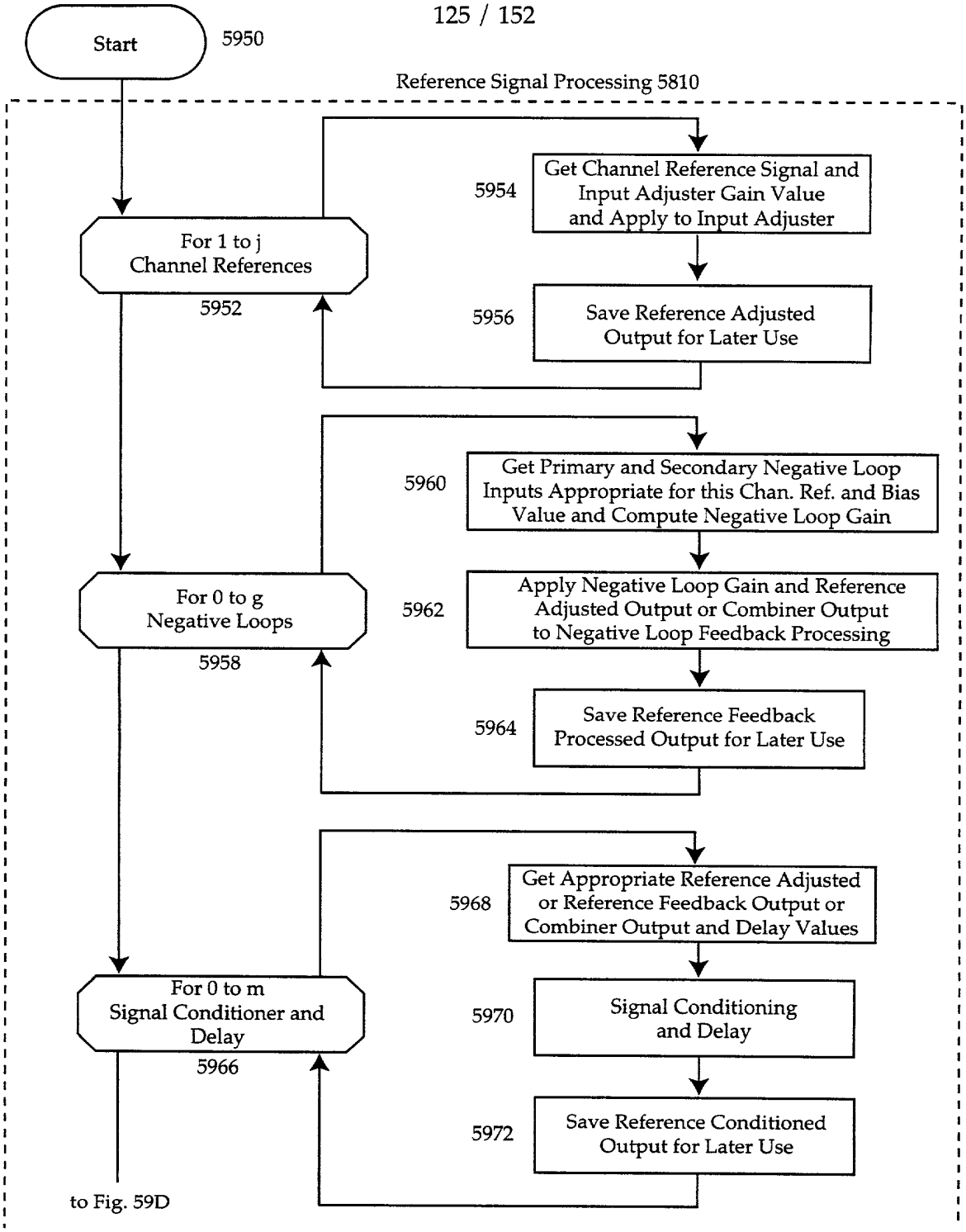

Start
5950
Reference Signal Processing 5810
For 1 to j
Channel References
5952
5954
Get Channel Reference Signal and Input Adjuster Gain Value and Apply to Input Adjuster
5956
Save Reference Adjusted Output for Later Use
For 0 to g
Negative Loops
5958
5960
Get Primary and Secondary Negative Loop Inputs Appropriate for this Chan. Ref. and Bias Value and Compute Negative Loop Gain
5962
Apply Negative Loop Gain and Reference Adjusted Output or Combiner Output to Negative Loop Feedback Processing
5964
Save Reference Feedback Processed Output for Later Use
For 0 to m
Signal Conditioner and Delay
5966
5968
Get Appropriate Reference Adjusted or Reference Feedback Output or Combiner Output and Delay Values
5970
Signal Conditioning and Delay
5972
Save Reference Conditioned Output for Later Use
to Fig. 59D

FIG. 59C

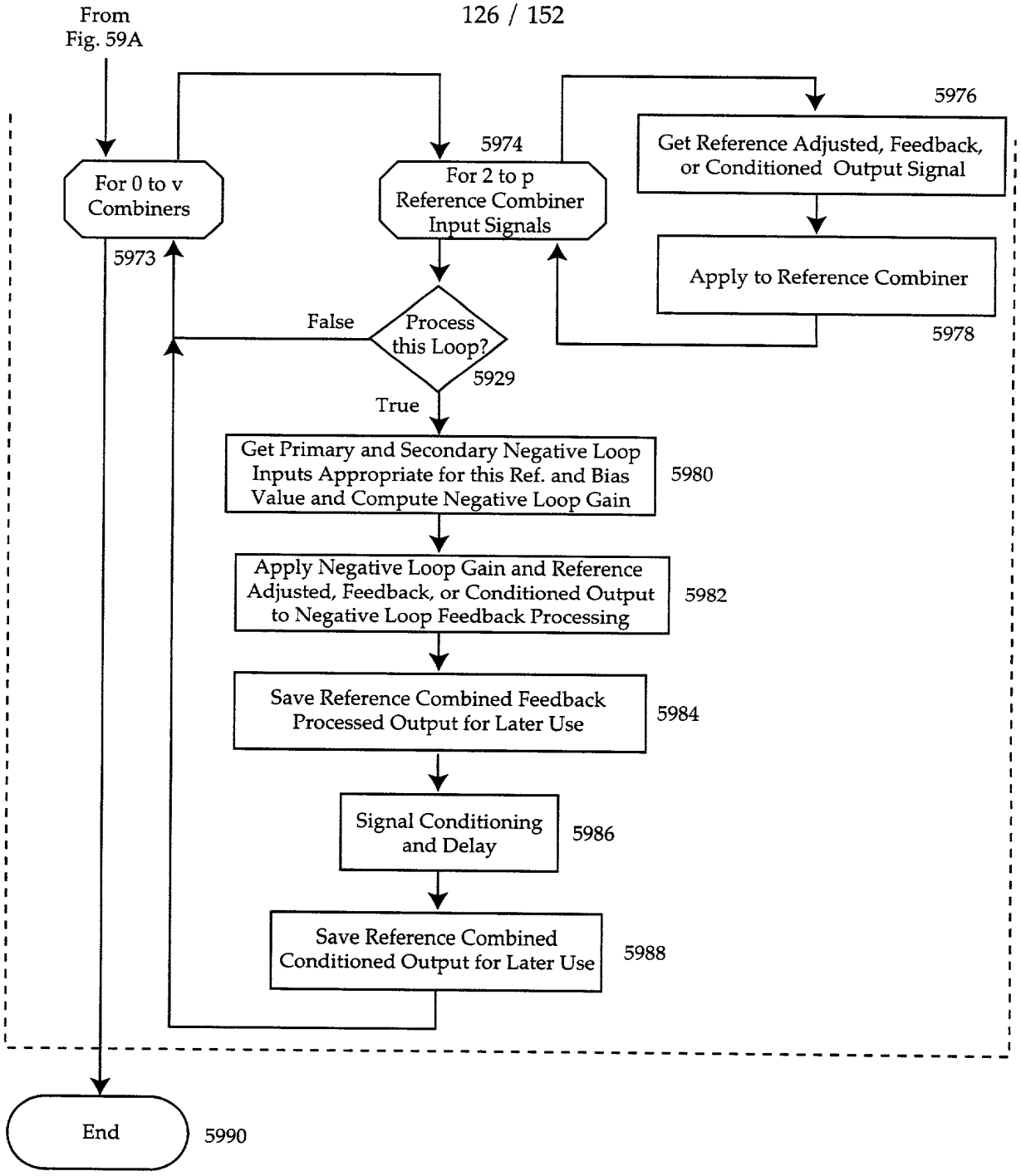

From Fig. 59A
For 0 to v Combiners
5973
5974
For 2 to p Reference Combiner Input Signals
5976
Get Reference Adjusted, Feedback, or Conditioned Output Signal
Apply to Reference Combiner
5978
False
Process this Loop?
5929
True
Get Primary and Secondary Negative Loop Inputs Appropriate for this Ref. and Bias Value and Compute Negative Loop Gain
5980
Apply Negative Loop Gain and Reference Adjusted, Feedback, or Conditioned Output to Negative Loop Feedback Processing
5982
Save Reference Combined Feedback Processed Output for Later Use
5984
Signal Conditioning and Delay
5986
Save Reference Combined Conditioned Output for Later Use
5988
End
5990

FIG. 59D

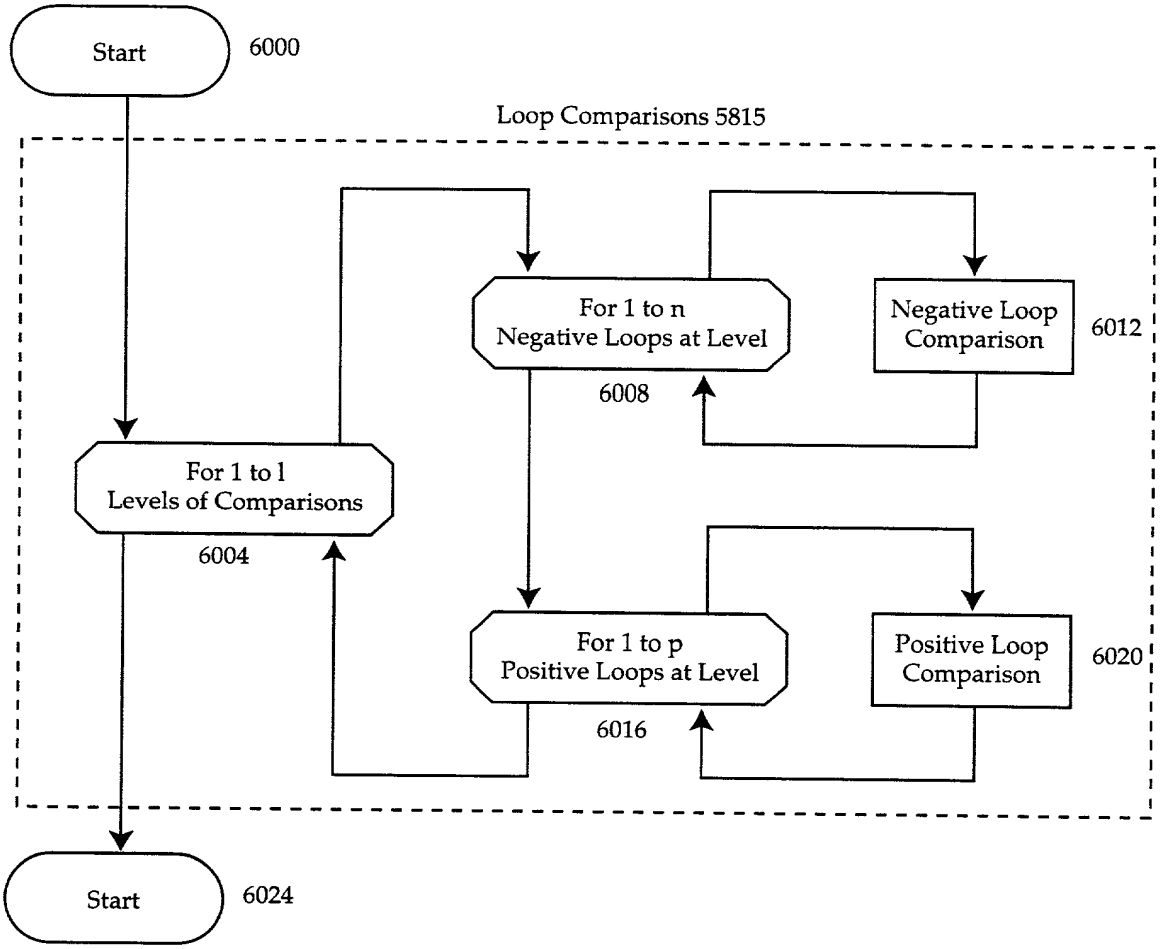

Start
6000
Loop Comparisons 5815
For 1 to n
Negative Loops at Level
6008
Negative Loop
Comparison
6012
For 1 to l
Levels of Comparisons
6004
For 1 to p
Positive Loops at Level
6016
Positive Loop
Comparison
6020
Start
6024

FIG. 60A

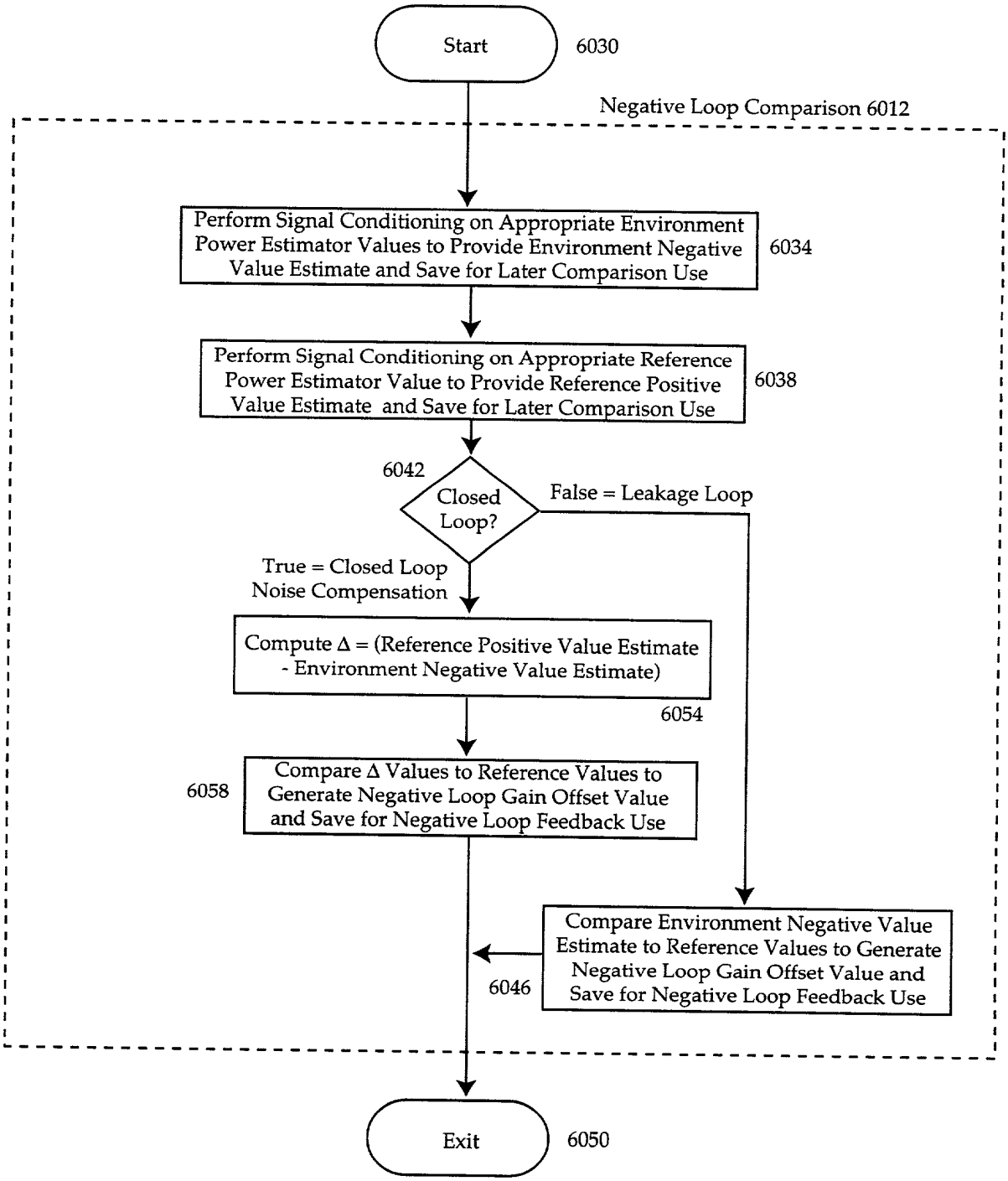

Start
6030
Negative Loop Comparison 6012
Perform Signal Conditioning on Appropriate Environment Power Estimator Values to Provide Environment Negative Value Estimate and Save for Later Comparison Use
6034
Perform Signal Conditioning on Appropriate Reference Power Estimator Value to Provide Reference Positive Value Estimate and Save for Later Comparison Use
6038
6042
Closed Loop?
False = Leakage Loop
True = Closed Loop Noise Compensation
Compute Δ = (Reference Positive Value Estimate - Environment Negative Value Estimate)
6054
6058
Compare Δ Values to Reference Values to Generate Negative Loop Gain Offset Value and Save for Negative Loop Feedback Use
Compare Environment Negative Value Estimate to Reference Values to Generate Negative Loop Gain Offset Value and Save for Negative Loop Feedback Use
6046
Exit
6050

FIG. 60B

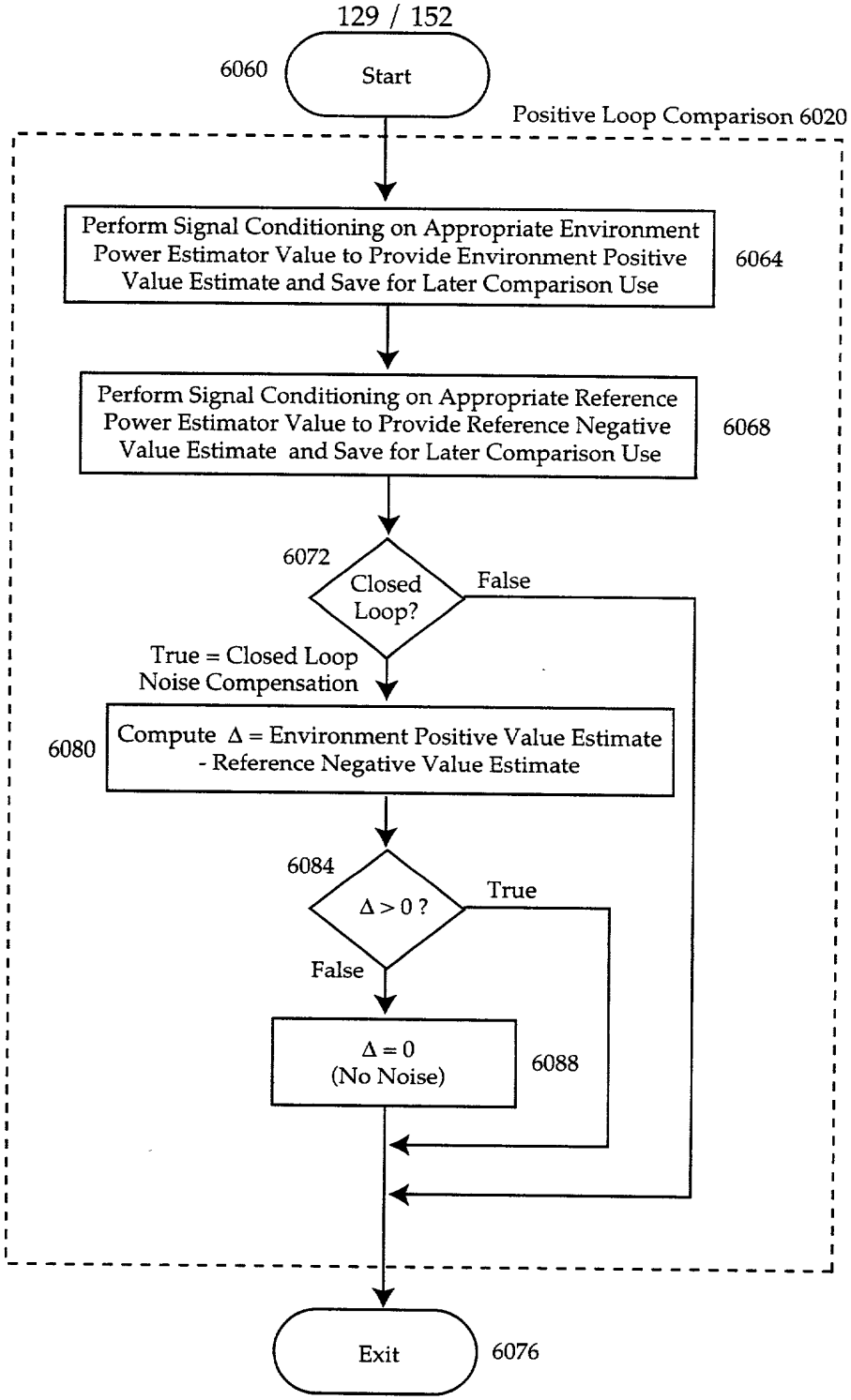

6060
Start
Positive Loop Comparison 6020
Perform Signal Conditioning on Appropriate Environment Power Estimator Value to Provide Environment Positive Value Estimate and Save for Later Comparison Use
6064
Perform Signal Conditioning on Appropriate Reference Power Estimator Value to Provide Reference Negative Value Estimate and Save for Later Comparison Use
6068
6072
Closed Loop?
False
True = Closed Loop Noise Compensation
6080
Compute Δ = Environment Positive Value Estimate - Reference Negative Value Estimate
6084
Δ > 0 ?
True
False
Δ = 0 (No Noise)
6088
Exit
6076

FIG. 60C

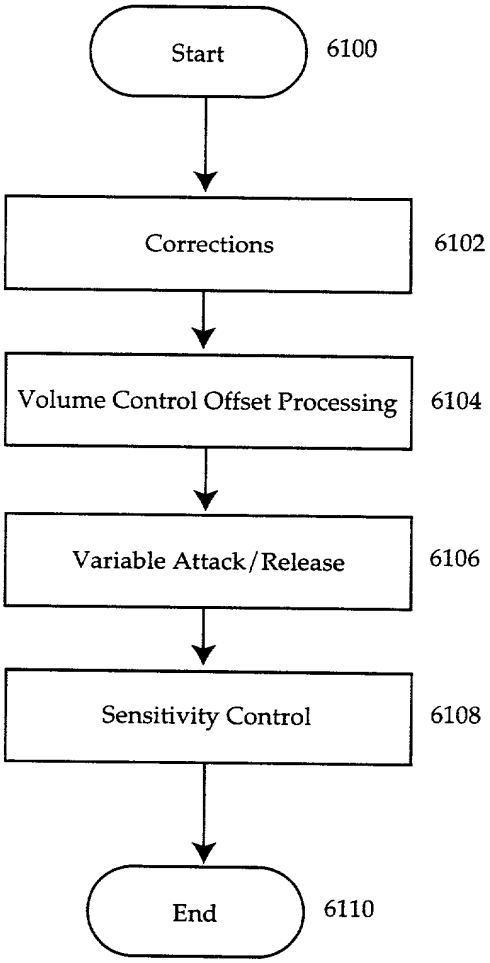

Start
6100
Corrections
6102
Volume Control Offset Processing
6104
Variable Attack/Release
6106
Sensitivity Control
6108
End
6110

FIG. 61A

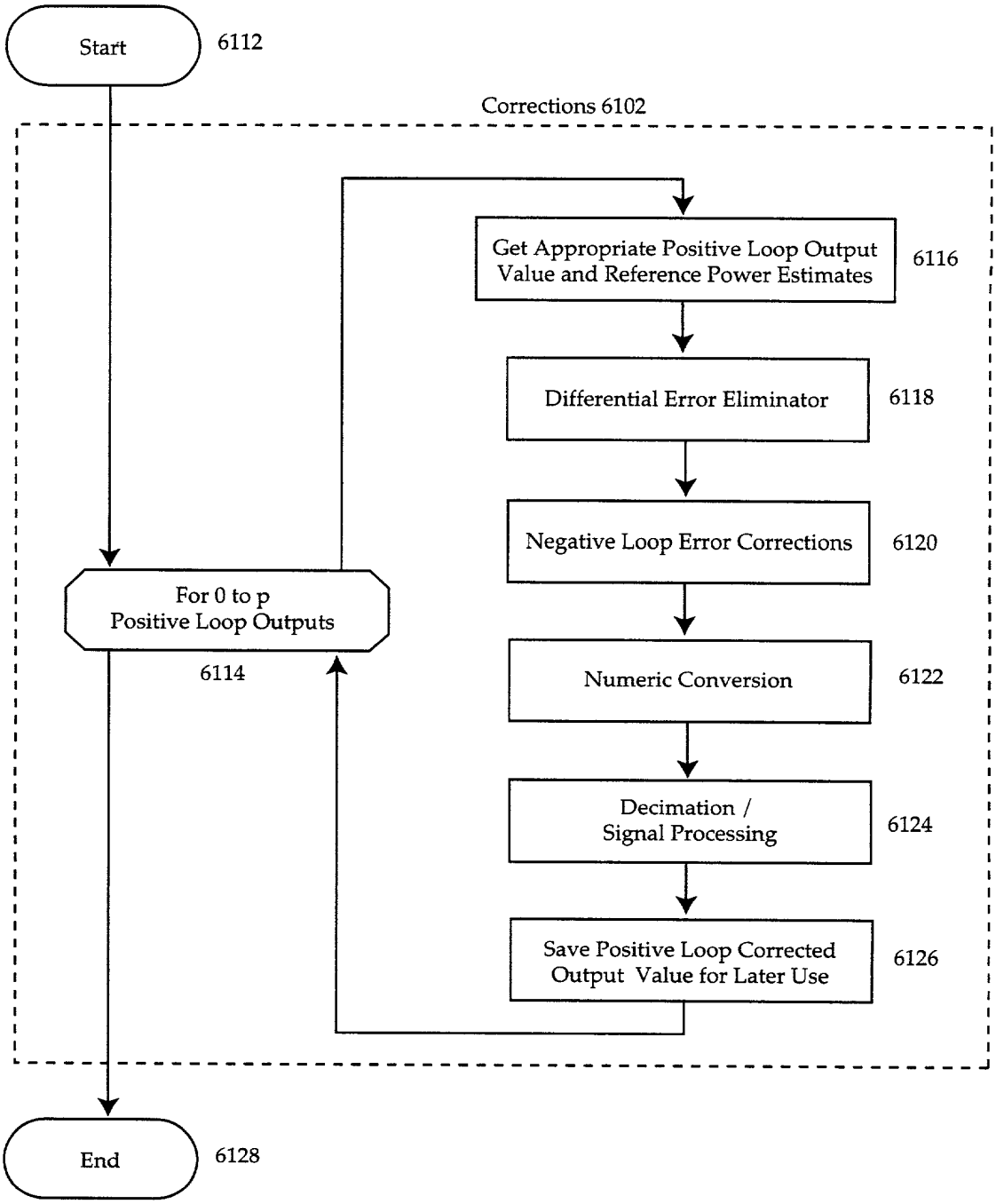

Start
6112
Corrections 6102
Get Appropriate Positive Loop Output Value and Reference Power Estimates
6116
Differential Error Eliminator
6118
Negative Loop Error Corrections
6120
For 0 to p Positive Loop Outputs
6114
Numeric Conversion
6122
Decimation / Signal Processing
6124
Save Positive Loop Corrected Output Value for Later Use
6126
End
6128

FIG. 61B

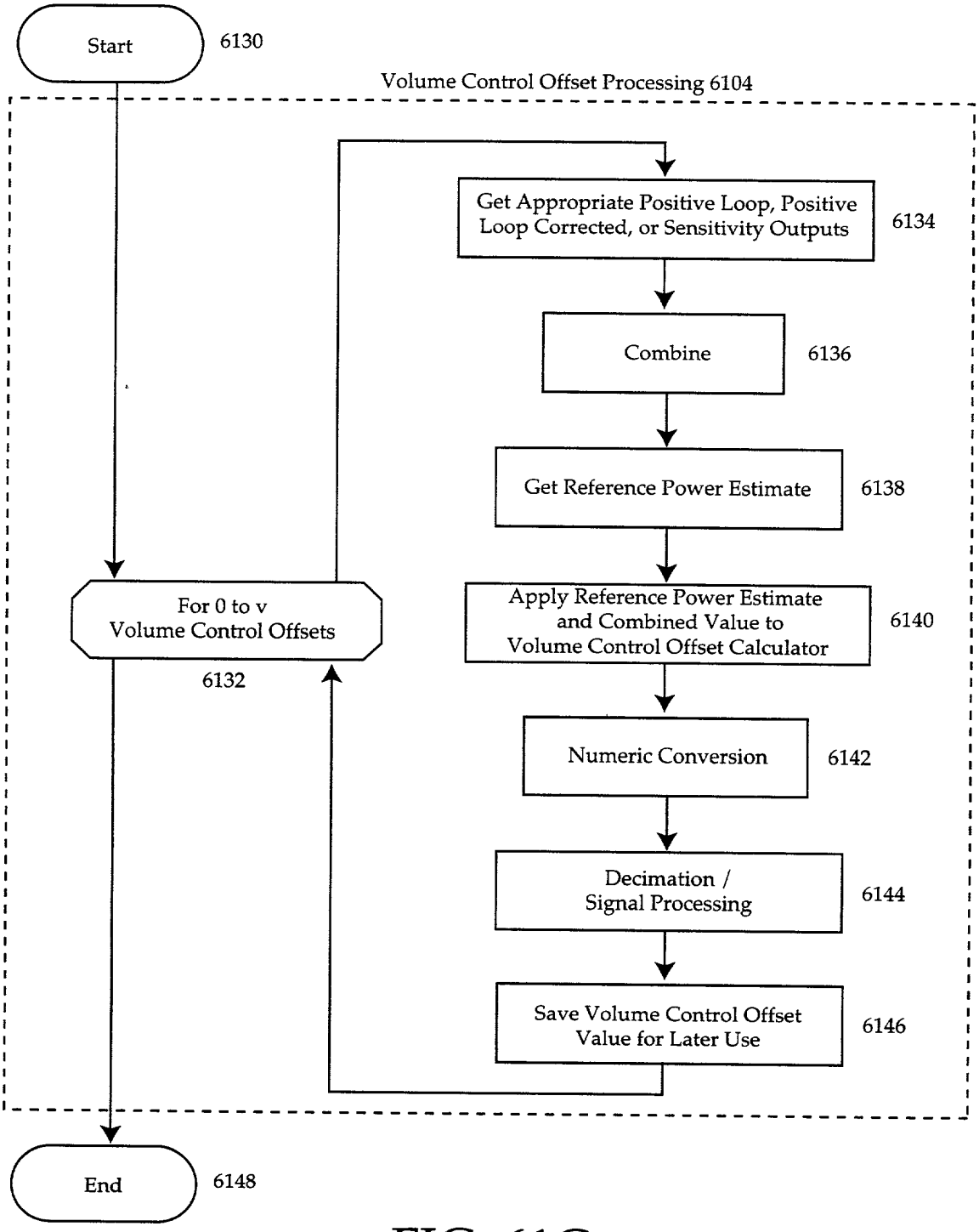

Start
6130
Volume Control Offset Processing 6104
Get Appropriate Positive Loop, Positive Loop Corrected, or Sensitivity Outputs
6134
Combine
6136
Get Reference Power Estimate
6138
Apply Reference Power Estimate and Combined Value to Volume Control Offset Calculator
6140
Numeric Conversion
6142
Decimation / Signal Processing
6144
Save Volume Control Offset Value for Later Use
6146
For 0 to v Volume Control Offsets
6132
End
6148

FIG. 61C

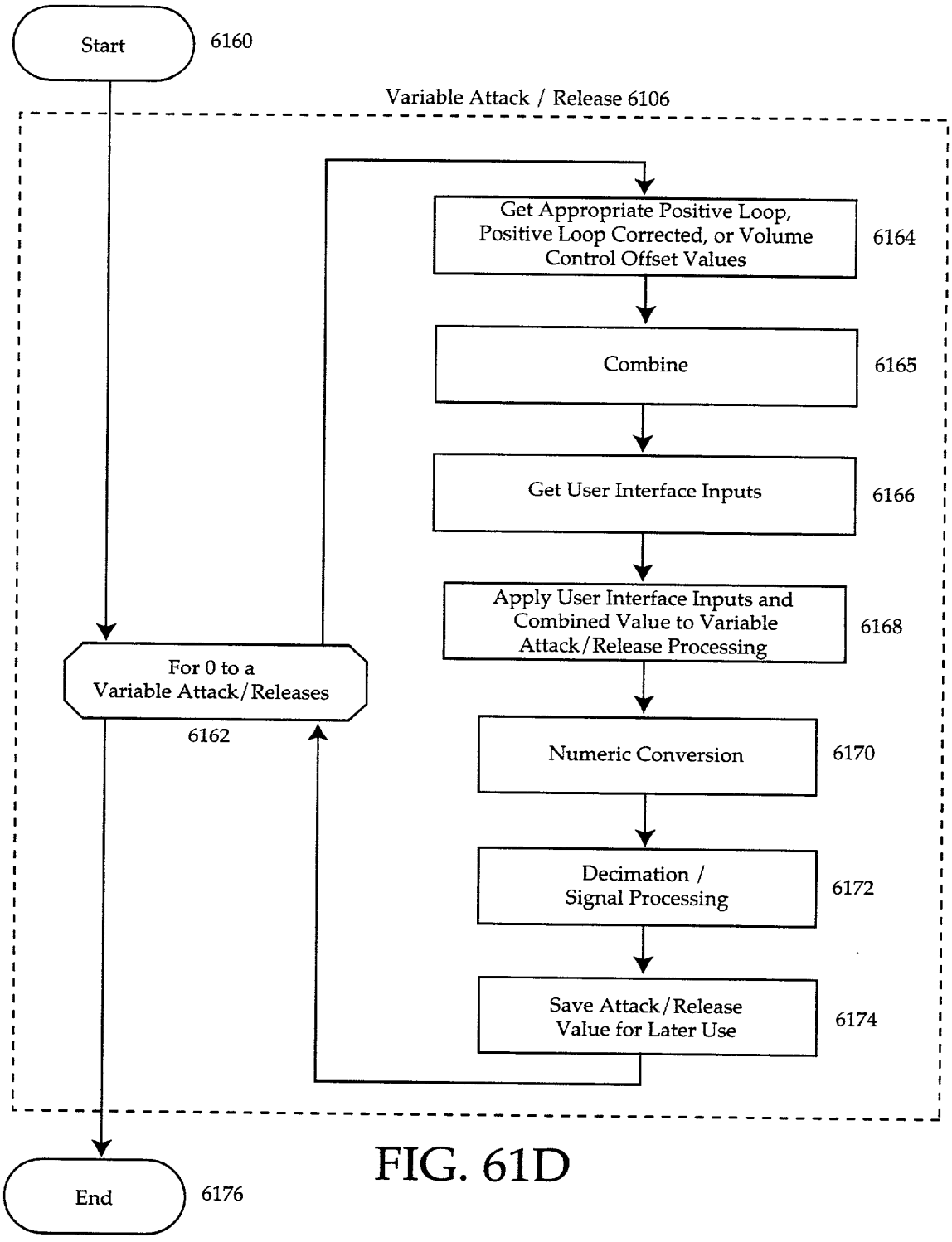

Start
6160
Variable Attack / Release 6106
Get Appropriate Positive Loop, Positive Loop Corrected, or Volume Control Offset Values
6164
Combine
6165
Get User Interface Inputs
6166
Apply User Interface Inputs and Combined Value to Variable Attack/Release Processing
6168
For 0 to a Variable Attack/Releases
6162
Numeric Conversion
6170
Decimation / Signal Processing
6172
Save Attack/Release Value for Later Use
6174
End
6176

FIG. 61D

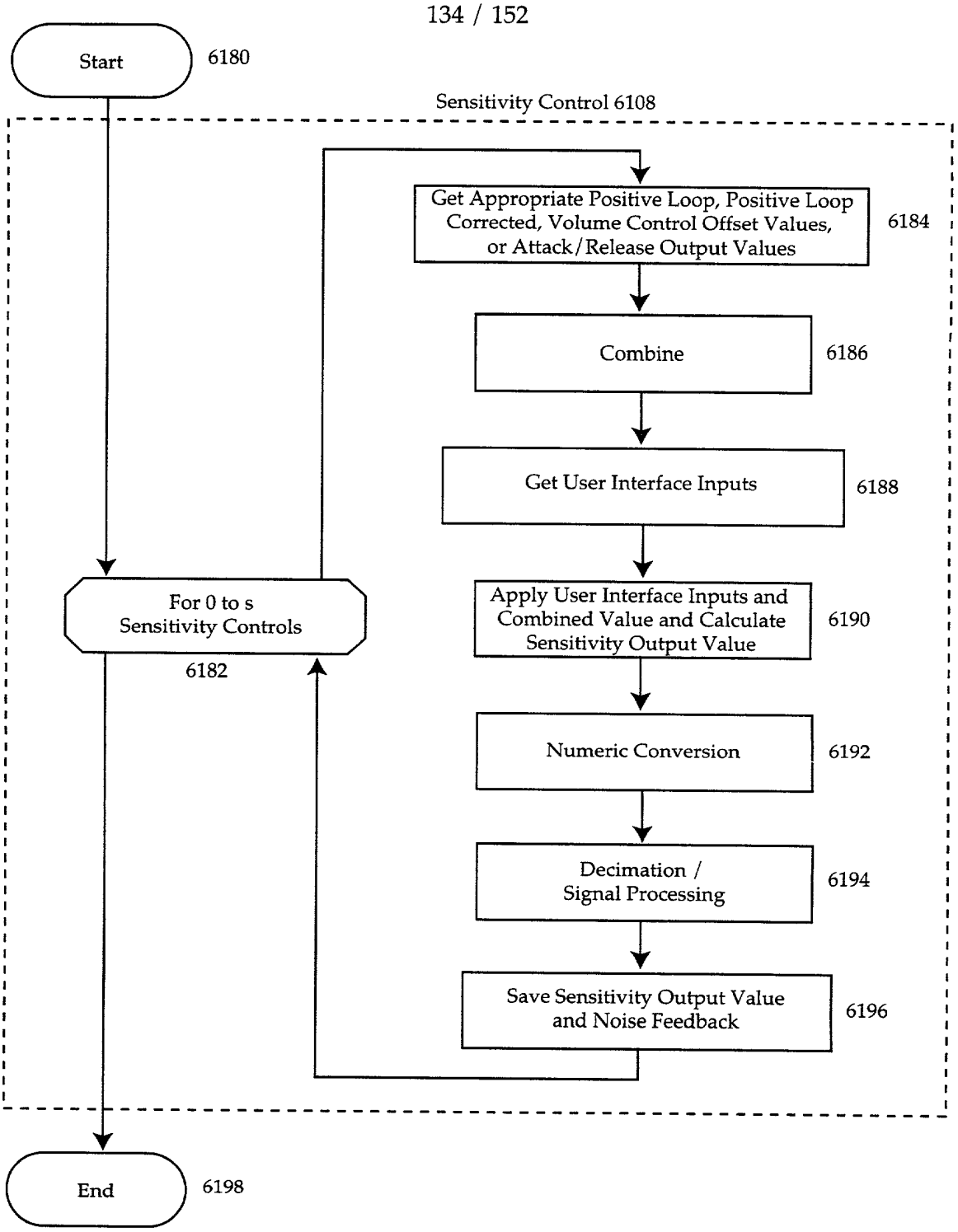

Start
6180
Sensitivity Control 6108
Get Appropriate Positive Loop, Positive Loop Corrected, Volume Control Offset Values, or Attack/Release Output Values
6184
Combine
6186
Get User Interface Inputs
6188
Apply User Interface Inputs and Combined Value and Calculate Sensitivity Output Value
6190
Numeric Conversion
6192
Decimation / Signal Processing
6194
Save Sensitivity Output Value and Noise Feedback
6196
For 0 to s Sensitivity Controls
6182
End
6198

FIG. 61E

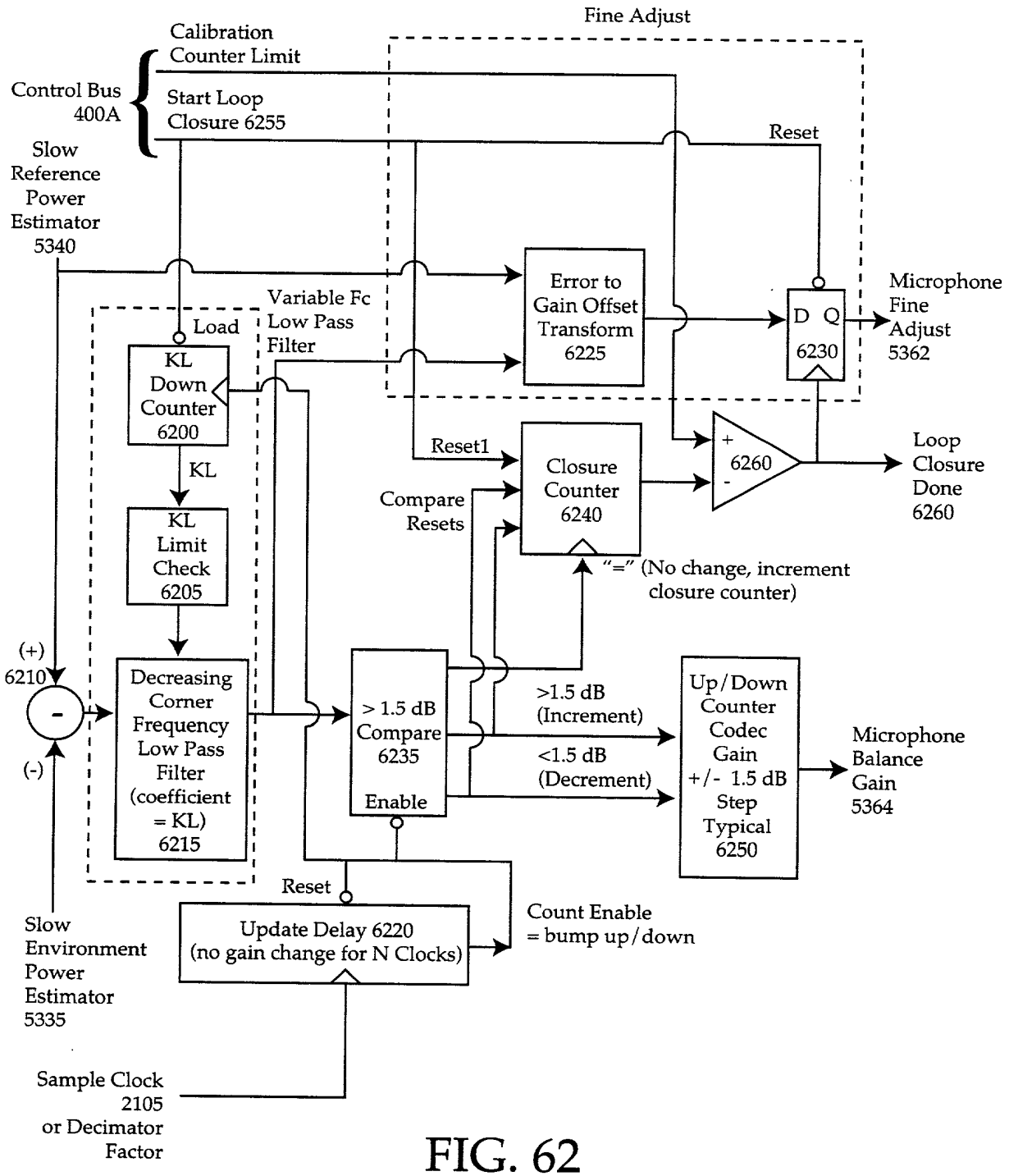

Fine Adjust
Calibration
Counter Limit
Control Bus
400A
Start Loop
Closure 6255
Reset
Slow
Reference
Power
Estimator
5340
Error to
Gain Offset
Transform
6225
D Q
6230
Microphone
Fine
Adjust
5362
Variable Fc
Low Pass
Filter
Load
KL
Down
Counter
6200
KL
KL
Limit
Check
6205
Reset1
Closure
Counter
6240
+
6260
-
Loop
Closure
Done
6260
Compare
Resets
"=" (No change, increment
closure counter)
(+)
6210
-
(-)
Decreasing
Corner
Frequency
Low Pass
Filter
(coefficient
= KL)
6215
> 1.5 dB
Compare
6235
Enable
>1.5 dB
(Increment)
<1.5 dB
(Decrement)
Up/Down
Counter
Codec
Gain
+/- 1.5 dB
Step
Typical
6250
Microphone
Balance
Gain
5364
Reset
Update Delay 6220
(no gain change for N Clocks)
Count Enable
= bump up/down
Slow
Environment
Power
Estimator
5335
Sample Clock
2105
or Decimator
Factor

FIG. 62

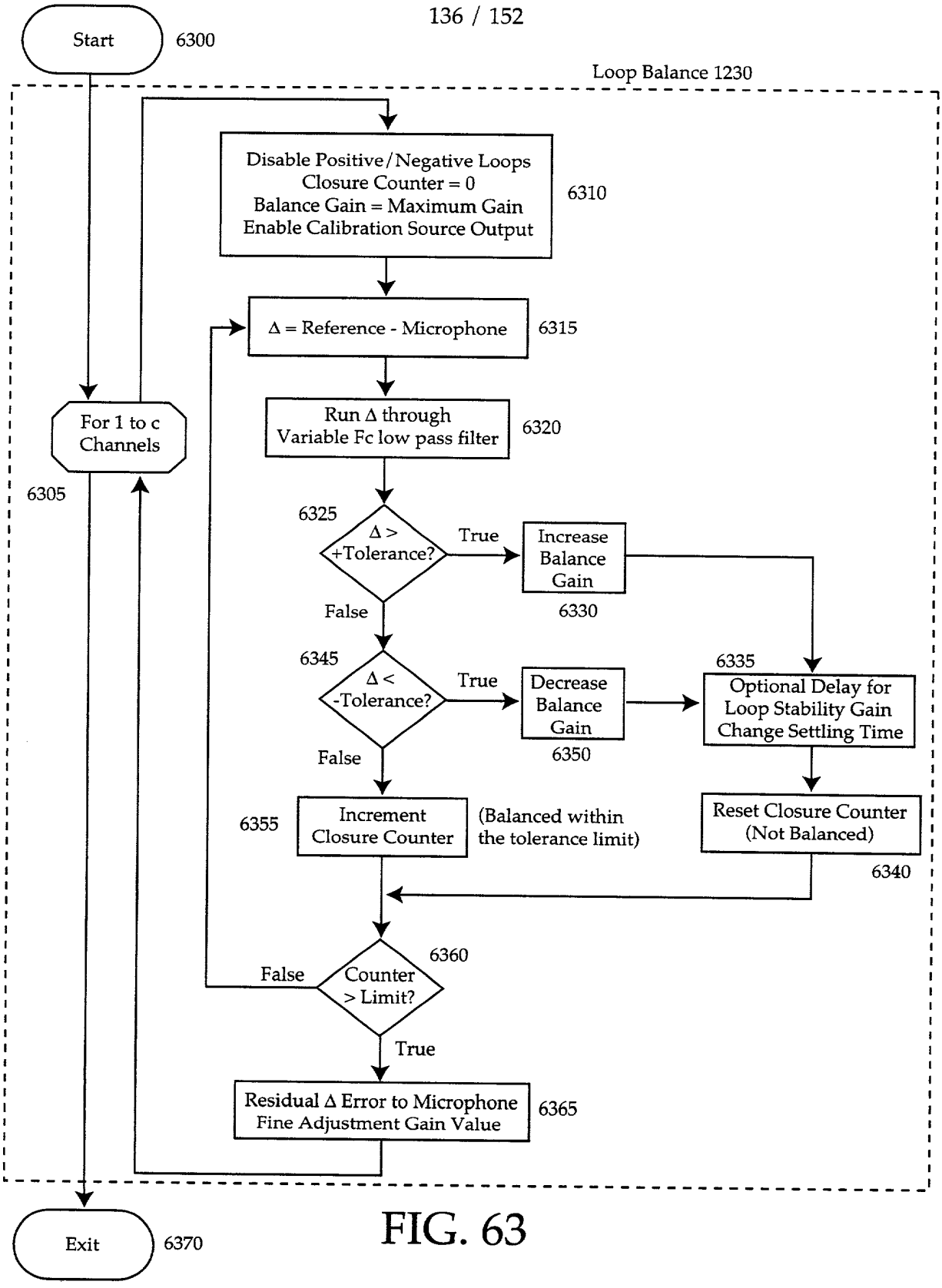

Start
6300
Loop Balance 1230
Disable Positive/Negative Loops
Closure Counter = 0
Balance Gain = Maximum Gain
Enable Calibration Source Output
6310
Δ = Reference - Microphone
6315
Run Δ through
Variable Fc low pass filter
6320
For 1 to c
Channels
6305
6325
Δ >
+Tolerance?
True
Increase
Balance
Gain
6330
False
6345
Δ <
-Tolerance?
True
Decrease
Balance
Gain
6350
6335
Optional Delay for
Loop Stability Gain
Change Settling Time
False
6355
Increment
Closure Counter
(Balanced within
the tolerance limit)
Reset Closure Counter
(Not Balanced)
6340
6360
False
Counter
> Limit?
True
Residual Δ Error to Microphone
Fine Adjustment Gain Value
6365
Exit
6370

FIG. 63

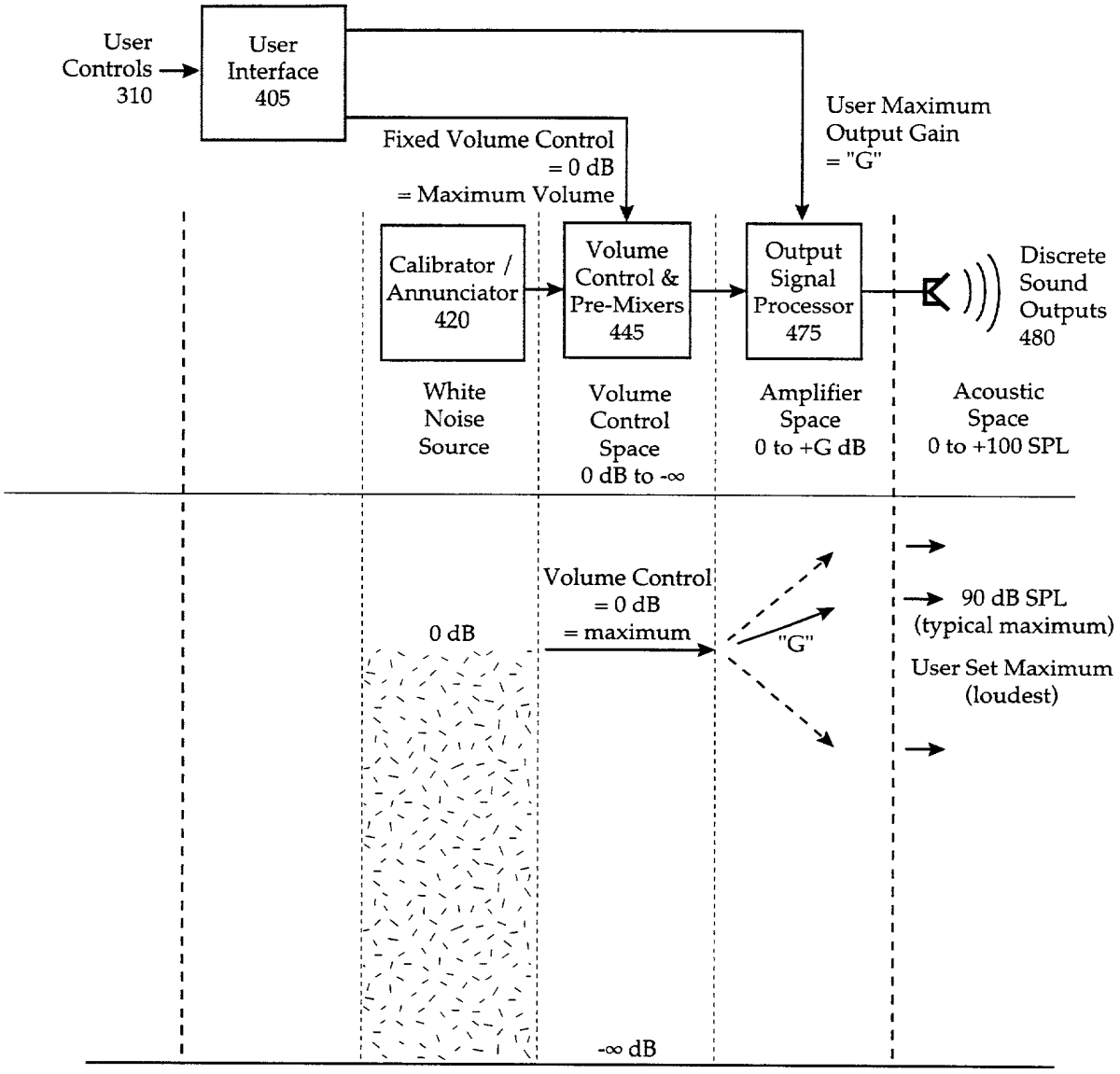

User Controls 310
User Interface 405
User Maximum Output Gain = "G"
Fixed Volume Control = 0 dB = Maximum Volume
Calibrator / Annunciator 420
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
White Noise Source
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
Volume Control = 0 dB = maximum
0 dB
"G"
90 dB SPL (typical maximum)
User Set Maximum (loudest)
-∞ dB

FIG. 64

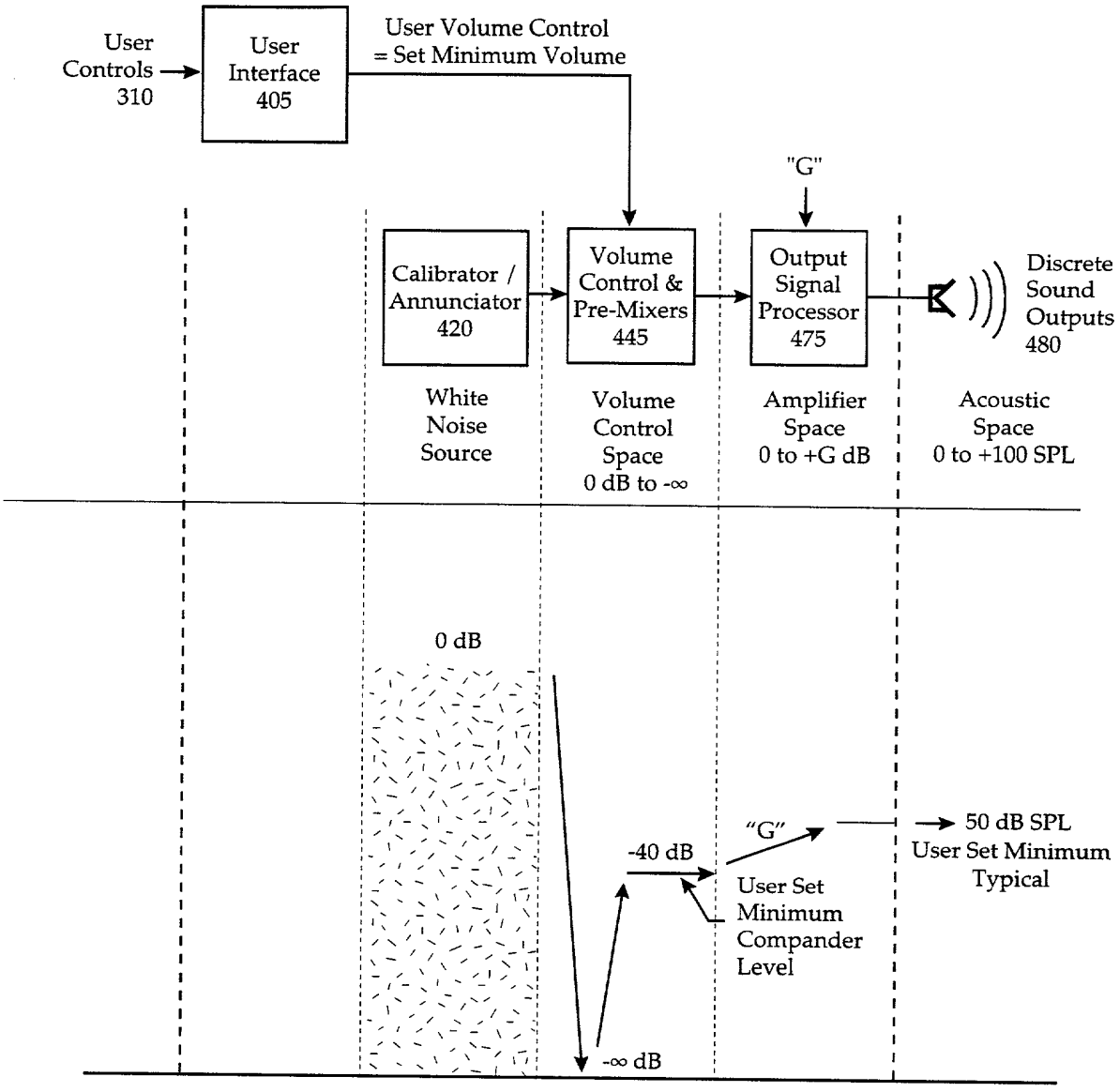

User Controls 310
User Interface 405
User Volume Control = Set Minimum Volume
"G"
Calibrator / Annunciator 420
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
White Noise Source
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
0 dB
-40 dB
"G"
50 dB SPL User Set Minimum Typical
User Set Minimum Compander Level
-∞ dB

FIG. 65

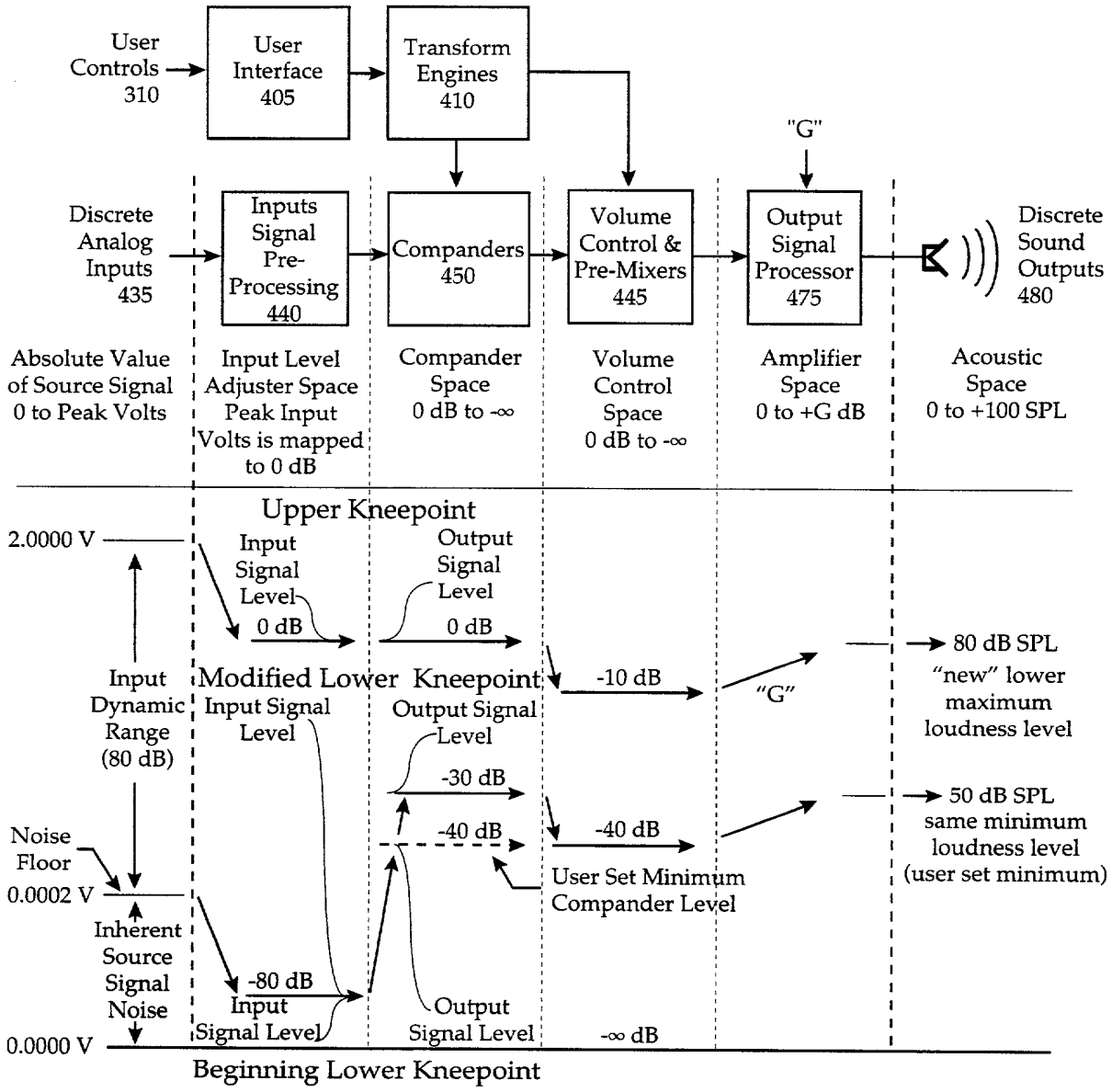

User Controls 310
User Interface 405
Transform Engines 410
"G"
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
Upper Kneepoint
2.0000 V
Input Signal Level
0 dB
Output Signal Level
0 dB
-10 dB
"G"
80 dB SPL
"new" lower maximum loudness level
Input Dynamic Range (80 dB)
Modified Lower Kneepoint
Input Signal Level
Output Signal Level
-30 dB
-40 dB
-40 dB
50 dB SPL
same minimum loudness level (user set minimum)
Noise Floor
0.0002 V
User Set Minimum Compander Level
Inherent Source Signal Noise
-80 dB
Input Signal Level
Output Signal Level
-∞ dB
0.0000 V
Beginning Lower Kneepoint

FIG. 66

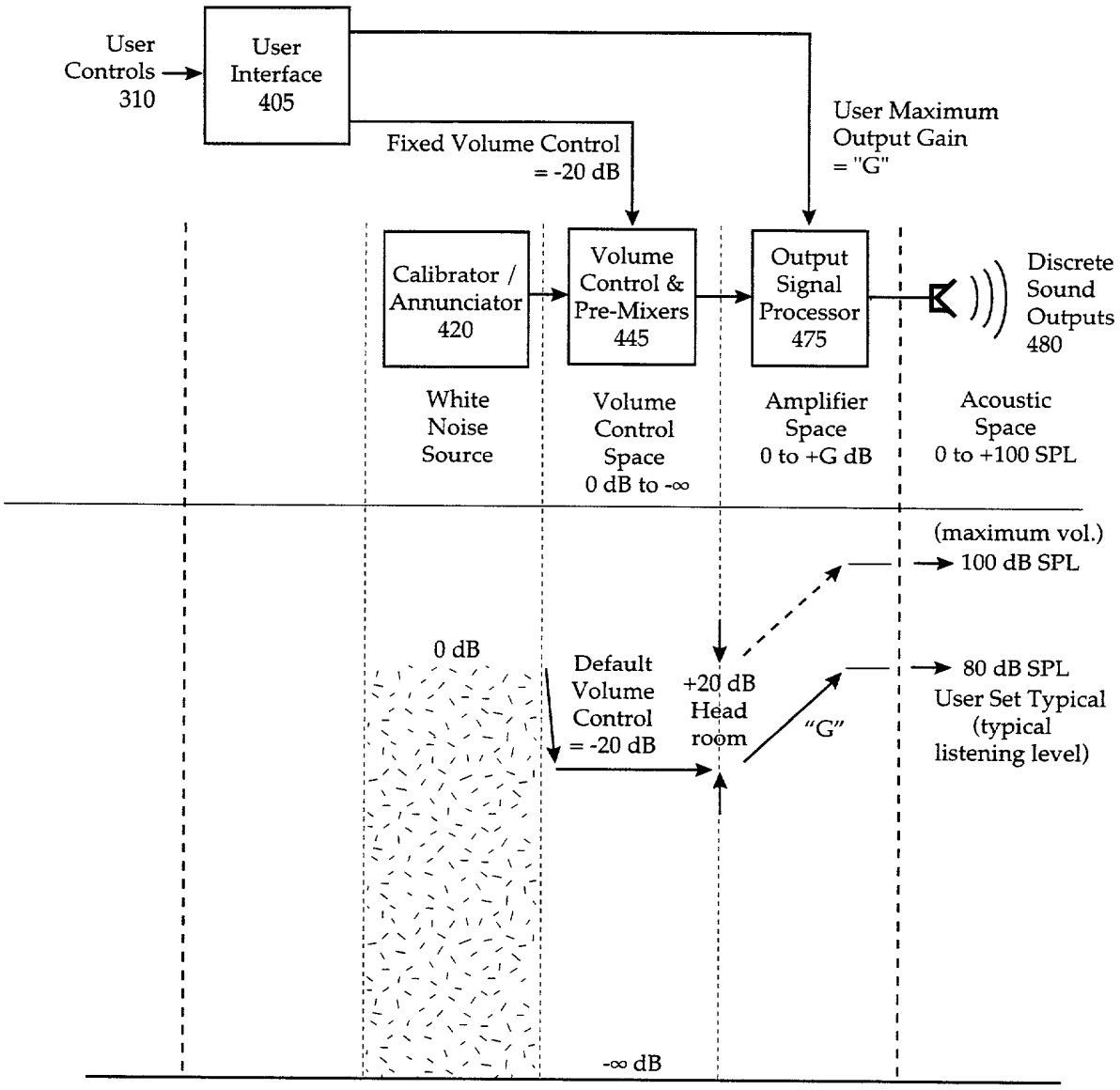

User Controls 310
User Interface 405
Fixed Volume Control = -20 dB
User Maximum Output Gain = "G"
Calibrator / Annunciator 420
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
White Noise Source
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
(maximum vol.)
100 dB SPL
0 dB
Default Volume Control = -20 dB
+20 dB Head room
"G"
80 dB SPL
User Set Typical (typical listening level)
-∞ dB

FIG. 67

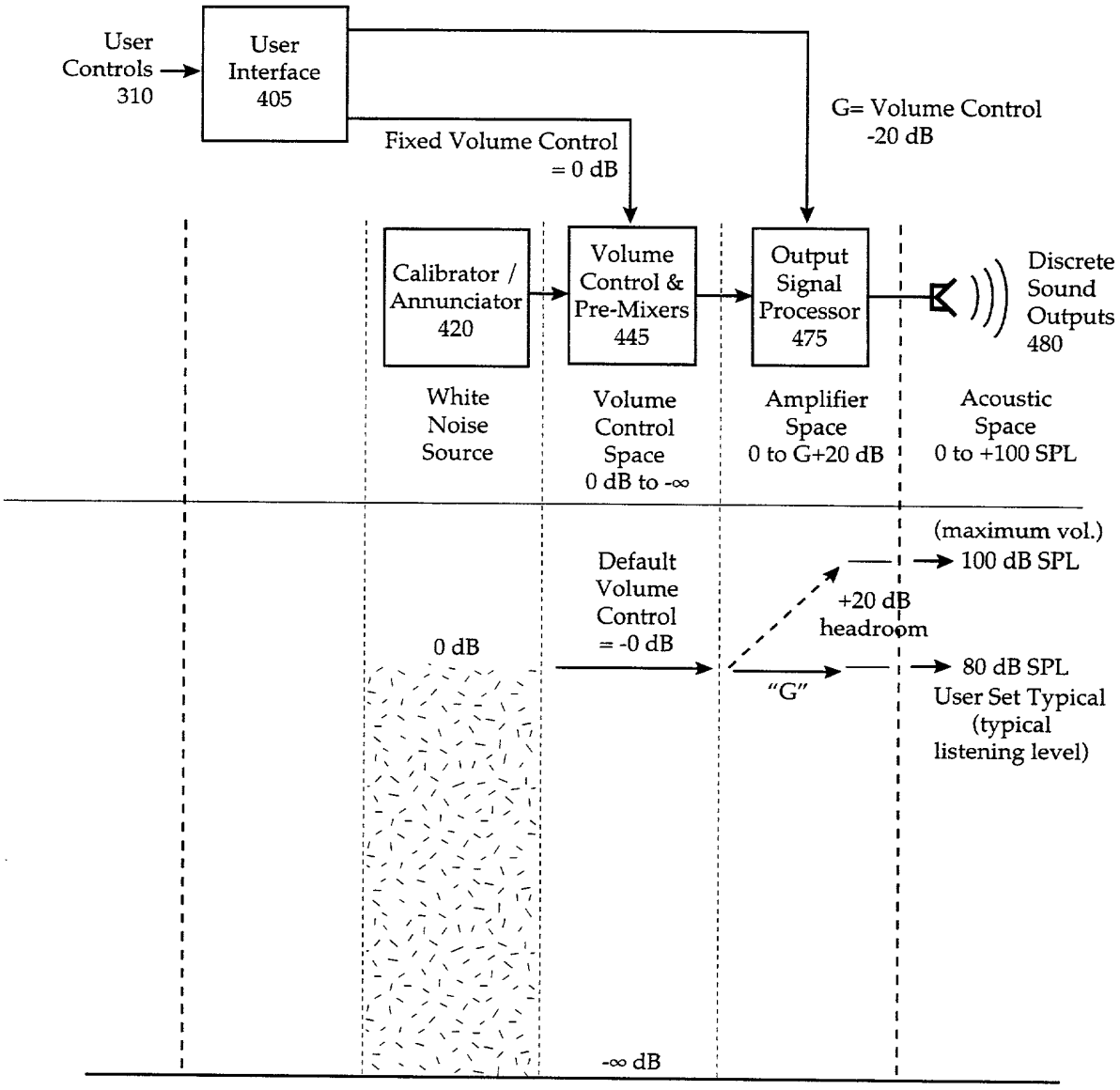

User Controls 310
User Interface 405
G= Volume Control -20 dB
Fixed Volume Control = 0 dB
Calibrator / Annunciator 420
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
White Noise Source
Volume Control Space 0 dB to -∞
Amplifier Space 0 to G+20 dB
Acoustic Space 0 to +100 SPL
(maximum vol.)
100 dB SPL
Default Volume Control = -0 dB
+20 dB headroom
0 dB
"G"
80 dB SPL
User Set Typical (typical listening level)
-∞ dB

FIG. 68

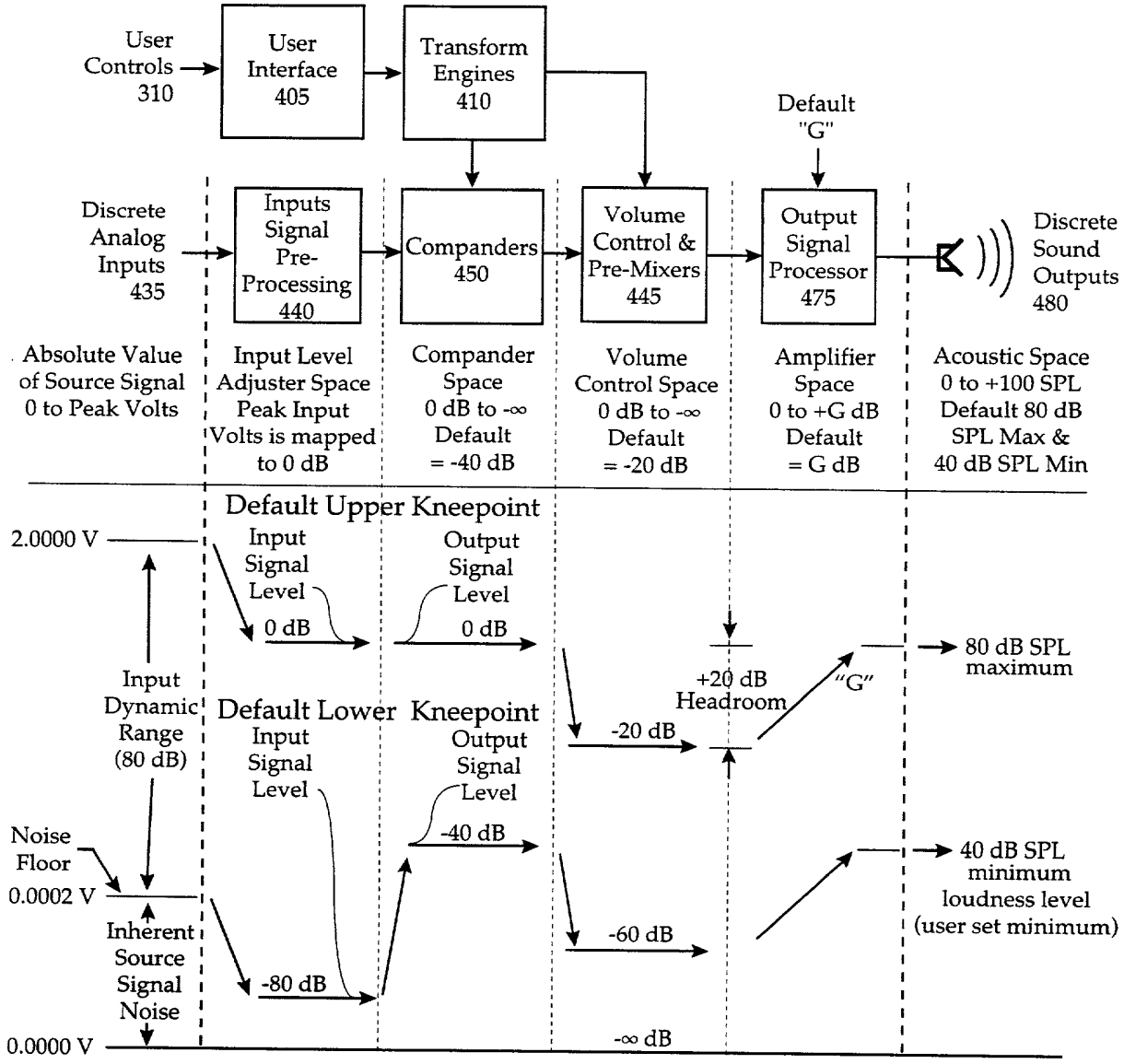

User Controls 310
User Interface 405
Transform Engines 410
Default "G"
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞ Default = -40 dB
Volume Control Space 0 dB to -∞ Default = -20 dB
Amplifier Space 0 to +G dB Default = G dB
Acoustic Space 0 to +100 SPL Default 80 dB SPL Max & 40 dB SPL Min
Default Upper Kneepoint
2.0000 V
Input Signal Level
0 dB
Output Signal Level
0 dB
+20 dB Headroom
"G"
80 dB SPL maximum
Input Dynamic Range (80 dB)
Default Lower Kneepoint
Input Signal Level
Output Signal Level
-20 dB
-40 dB
Noise Floor
0.0002 V
Inherent Source Signal Noise
-80 dB
-60 dB
40 dB SPL minimum loudness level (user set minimum)
0.0000 V
-∞ dB

FIG. 69

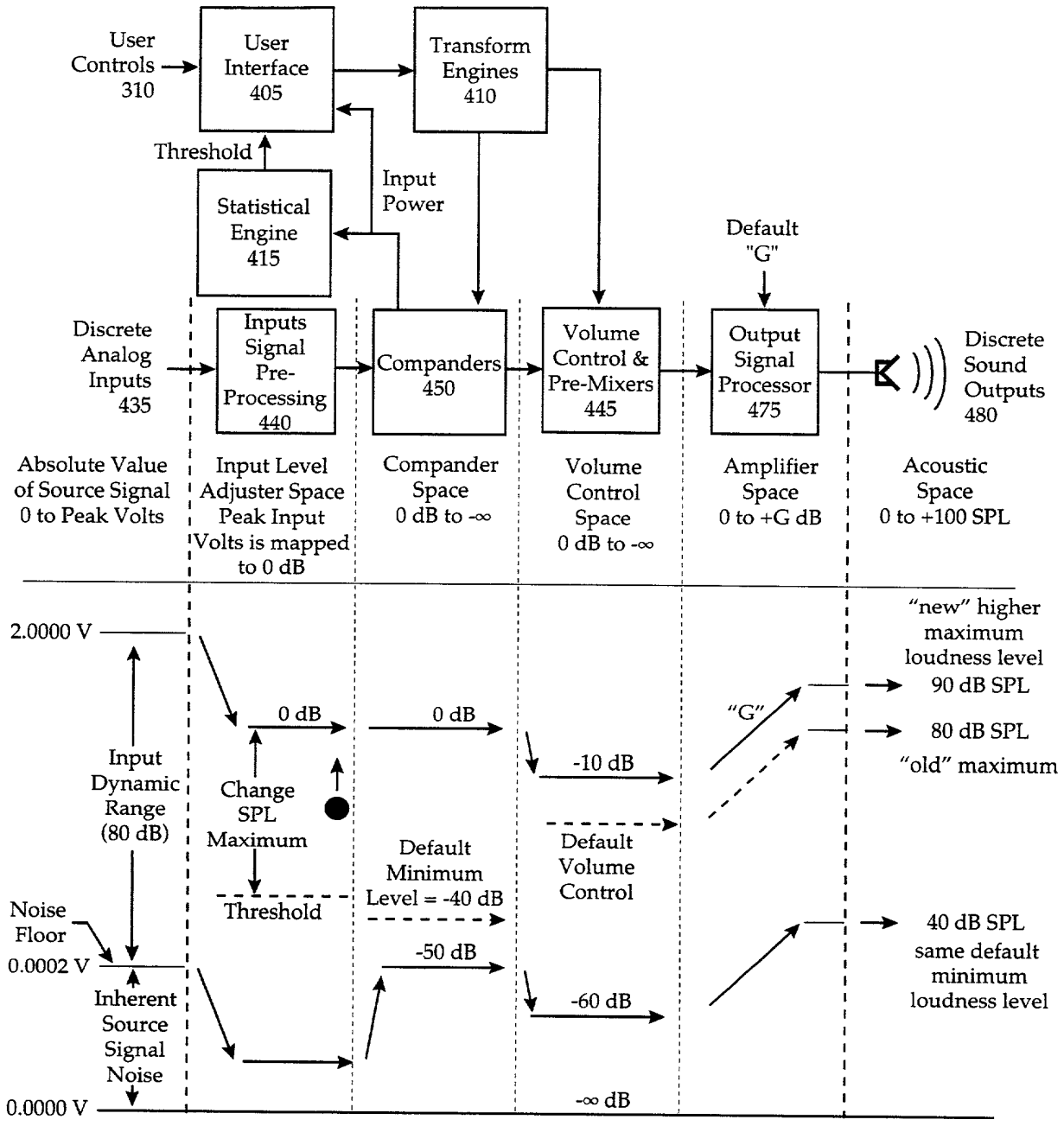

User Controls 310
User Interface 405
Transform Engines 410
Threshold
Statistical Engine 415
Input Power
Default "G"
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
2.0000 V
0 dB
0 dB
-10 dB
"G"
"new" higher maximum loudness level
90 dB SPL
80 dB SPL
"old" maximum
Input Dynamic Range (80 dB)
Change SPL Maximum
Default Minimum Level = -40 dB
Default Volume Control
Threshold
Noise Floor
0.0002 V
-50 dB
-60 dB
40 dB SPL
same default minimum loudness level
Inherent Source Signal Noise
0.0000 V
-∞ dB

FIG. 70

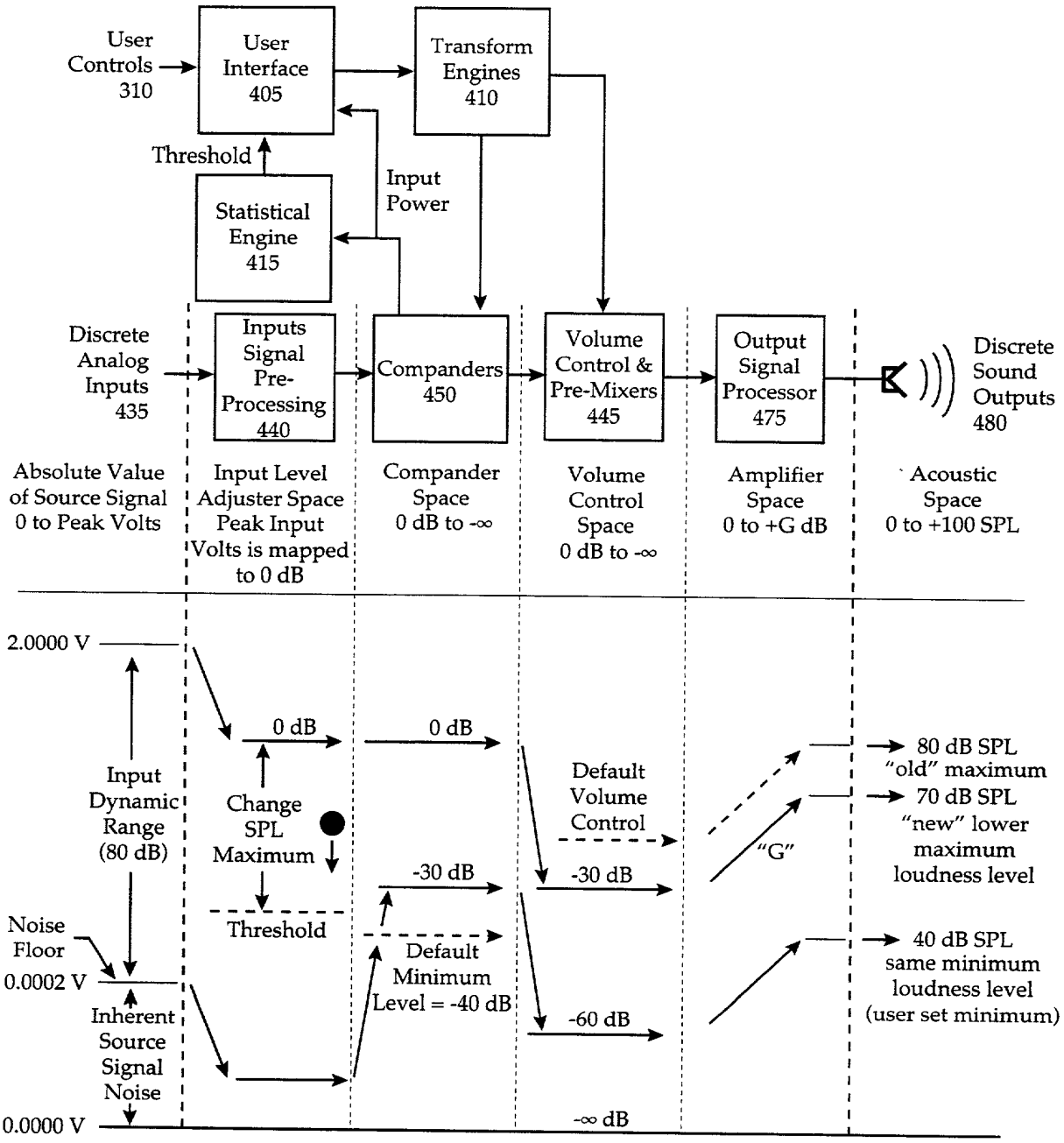

User Controls 310
User Interface 405
Transform Engines 410
Threshold
Statistical Engine 415
Input Power
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
2.0000 V
0 dB
0 dB
Input Dynamic Range (80 dB)
Change SPL Maximum
Default Volume Control
"G"
80 dB SPL "old" maximum
70 dB SPL "new" lower maximum loudness level
-30 dB
-30 dB
Threshold
Noise Floor
0.0002 V
Default Minimum Level = -40 dB
-60 dB
40 dB SPL same minimum loudness level (user set minimum)
Inherent Source Signal Noise
0.0000 V
-∞ dB

FIG. 71

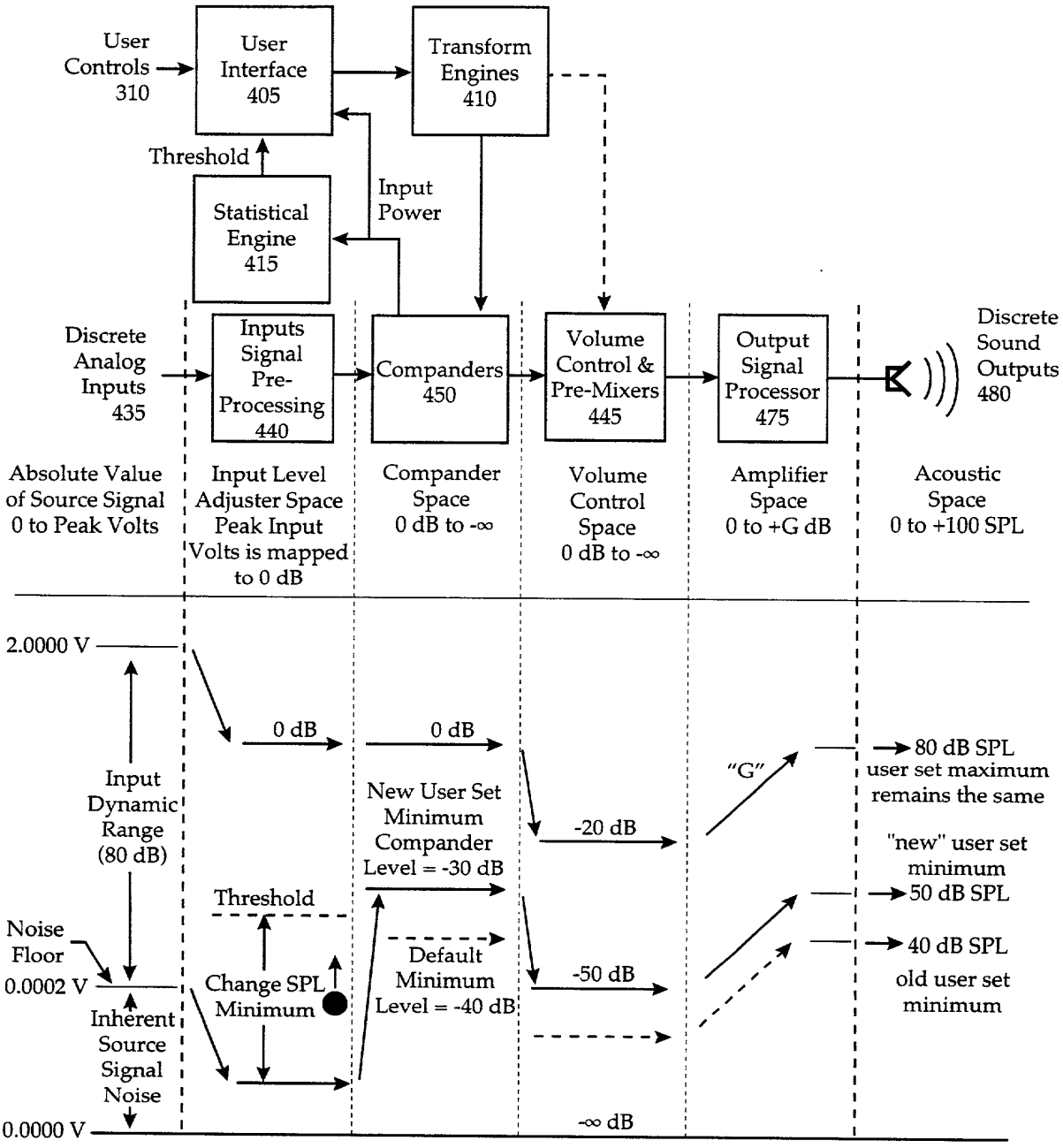

User Controls 310
User Interface 405
Transform Engines 410
Threshold
Statistical Engine 415
Input Power
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
2.0000 V
0 dB
0 dB
"G"
80 dB SPL
user set maximum
remains the same
Input Dynamic Range (80 dB)
New User Set Minimum Compander Level = -30 dB
-20 dB
"new" user set minimum
50 dB SPL
Threshold
Noise Floor
0.0002 V
Change SPL Minimum
Default Minimum Level = -40 dB
-50 dB
40 dB SPL
old user set minimum
Inherent Source Signal Noise
0.0000 V
-∞ dB

FIG. 72

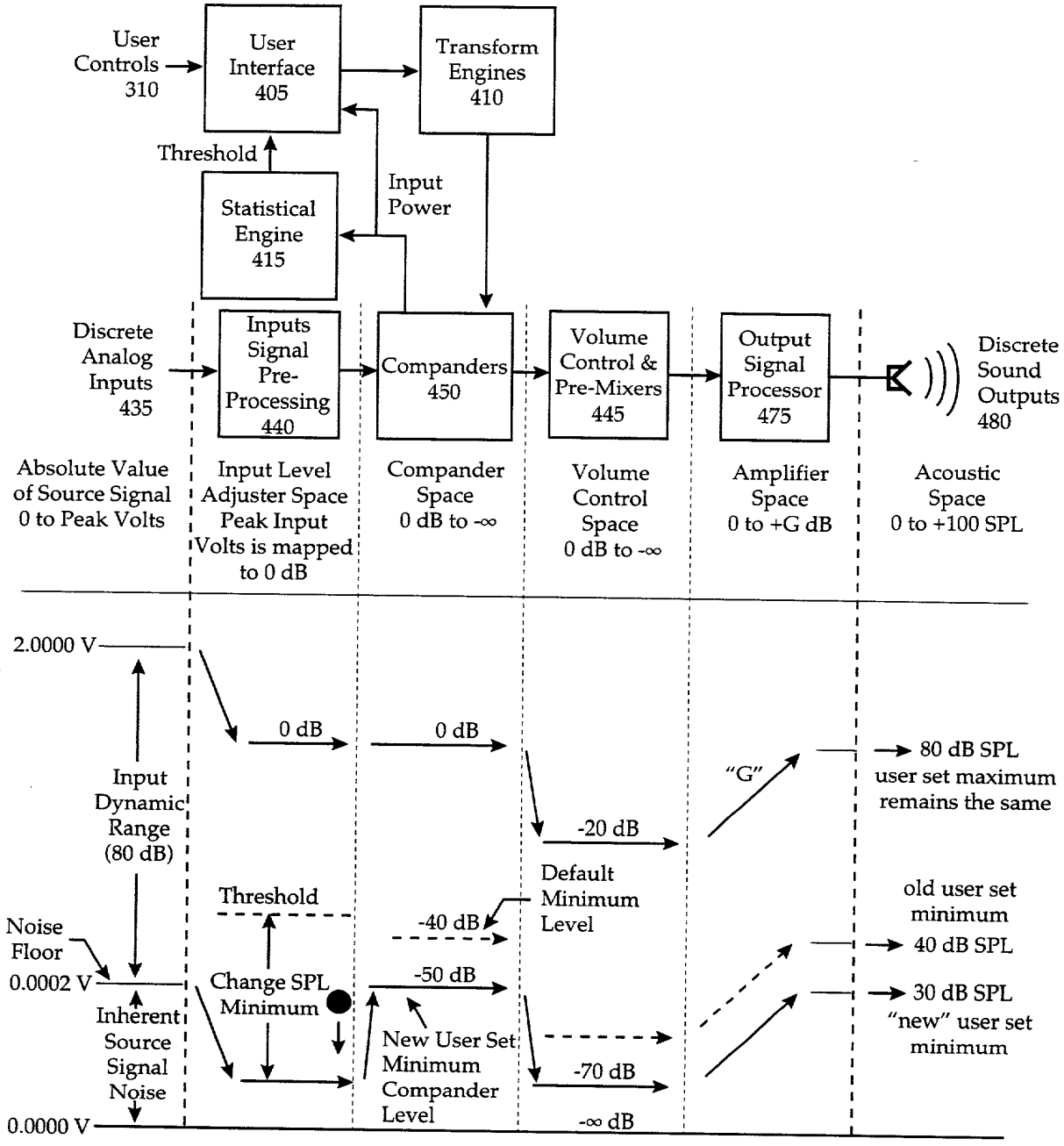

User Controls 310
User Interface 405
Transform Engines 410
Threshold
Statistical Engine 415
Input Power
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
2.0000 V
0 dB
0 dB
-20 dB
"G"
80 dB SPL
user set maximum
remains the same
Input Dynamic Range (80 dB)
Default Minimum Level
Threshold
-40 dB
old user set minimum
Noise Floor
0.0002 V
Change SPL Minimum
-50 dB
40 dB SPL
30 dB SPL
"new" user set minimum
Inherent Source Signal Noise
New User Set Minimum Compander Level
-70 dB
0.0000 V
-∞ dB

FIG. 73

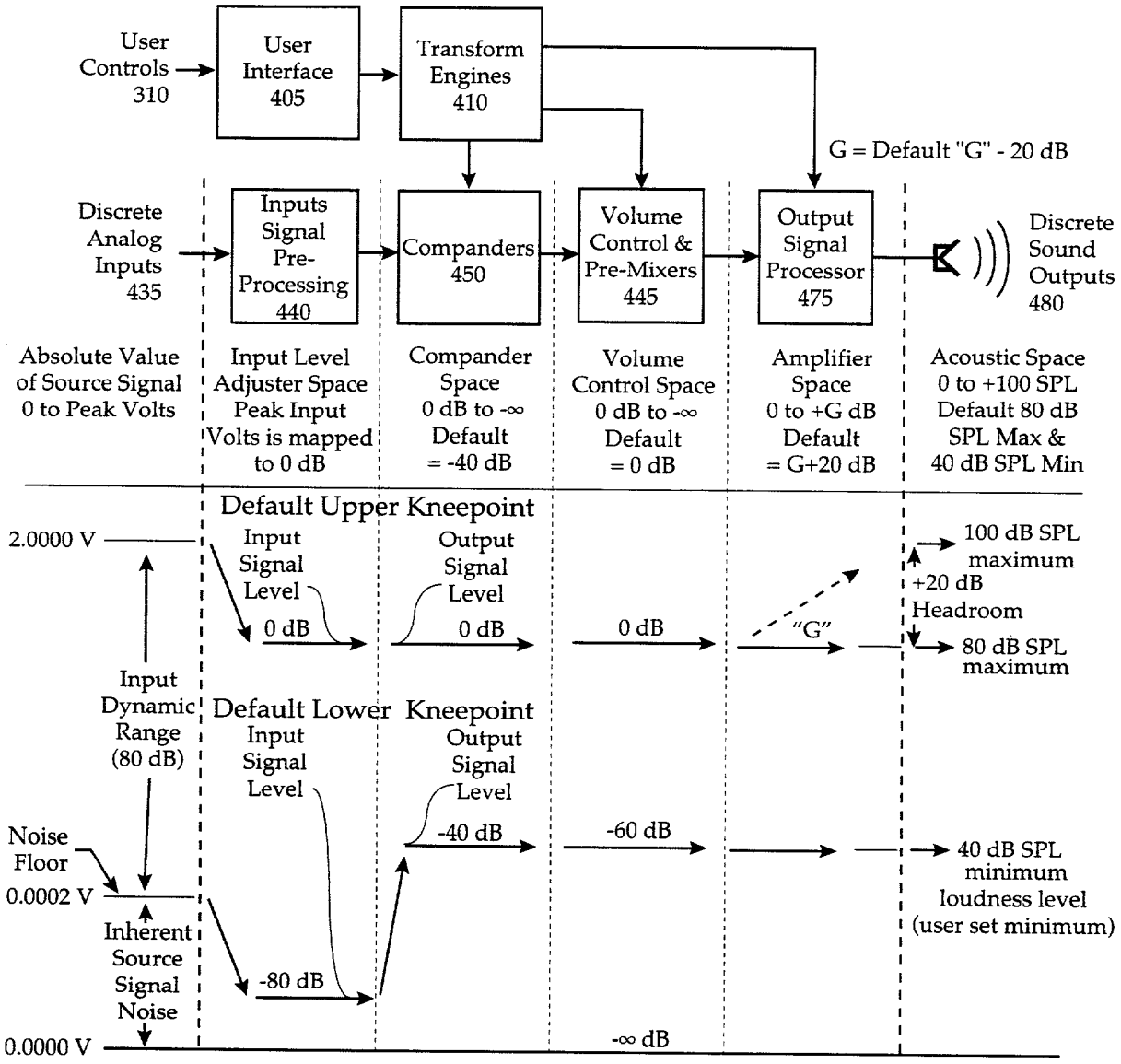

User Controls 310
User Interface 405
Transform Engines 410
G = Default "G" - 20 dB
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞ Default = -40 dB
Volume Control Space 0 dB to -∞ Default = 0 dB
Amplifier Space 0 to +G dB Default = G+20 dB
Acoustic Space 0 to +100 SPL Default 80 dB SPL Max & 40 dB SPL Min
Default Upper Kneepoint
2.0000 V
Input Signal Level
0 dB
Output Signal Level
0 dB
0 dB
"G"
100 dB SPL maximum
+20 dB Headroom
80 dB SPL maximum
Input Dynamic Range (80 dB)
Default Lower Kneepoint
Input Signal Level
Output Signal Level
-40 dB
-60 dB
Noise Floor
0.0002 V
Inherent Source Signal Noise
-80 dB
40 dB SPL minimum loudness level (user set minimum)
0.0000 V
-∞ dB

FIG. 74

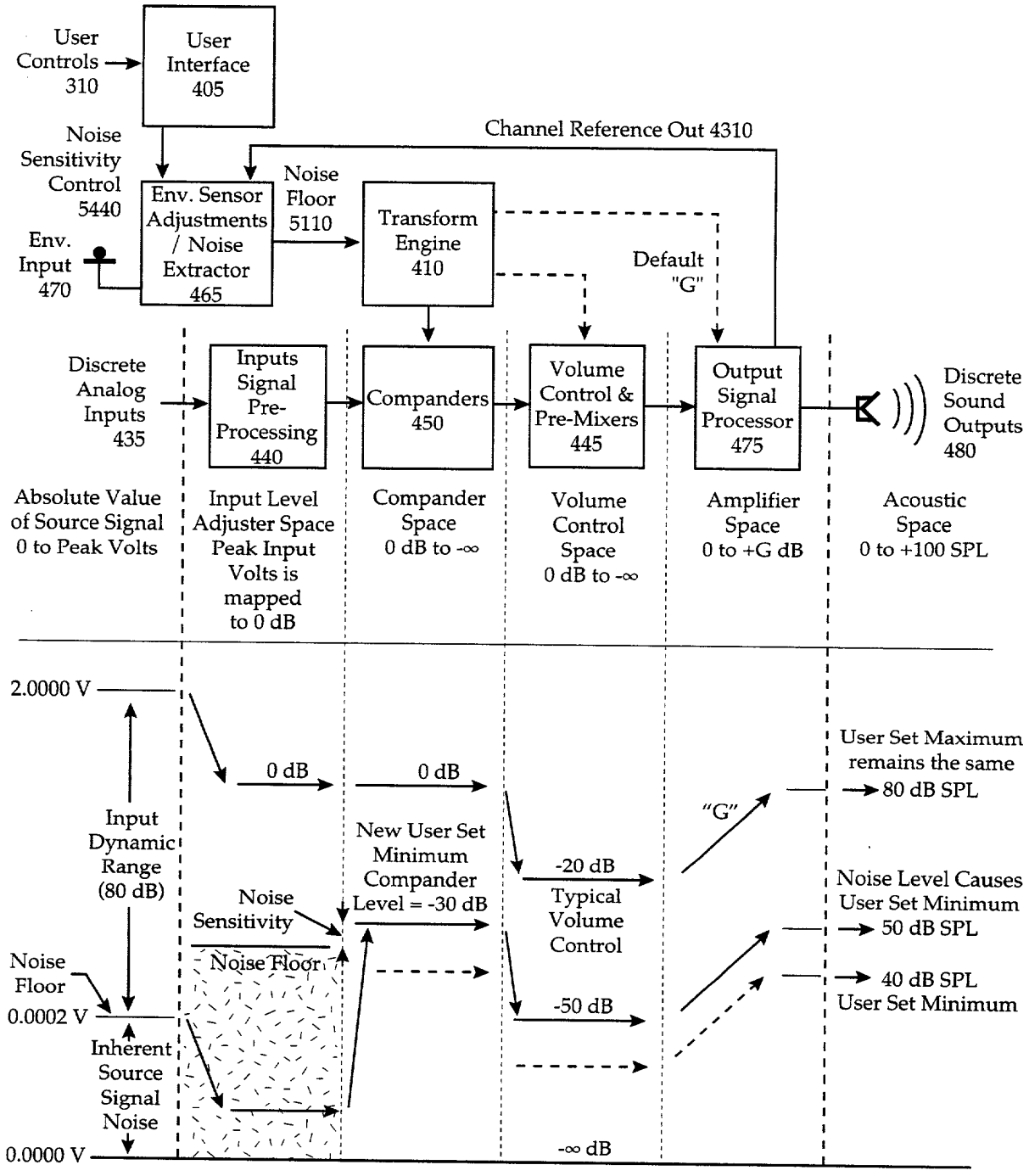

User Controls 310
User Interface 405
Noise Sensitivity Control 5440
Channel Reference Out 4310
Env. Input 470
Env. Sensor Adjustments / Noise Extractor 465
Noise Floor 5110
Transform Engine 410
Default "G"
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Companders 450
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Compander Space 0 dB to -∞
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB
Acoustic Space 0 to +100 SPL
2.0000 V
0 dB
0 dB
"G"
User Set Maximum remains the same
80 dB SPL
Input Dynamic Range (80 dB)
New User Set Minimum Compander Level = -30 dB
-20 dB
Typical Volume Control
Noise Level Causes User Set Minimum
50 dB SPL
Noise Sensitivity
Noise Floor
Noise Floor
0.0002 V
-50 dB
40 dB SPL
User Set Minimum
Inherent Source Signal Noise
0.0000 V
-∞ dB

FIG. 75

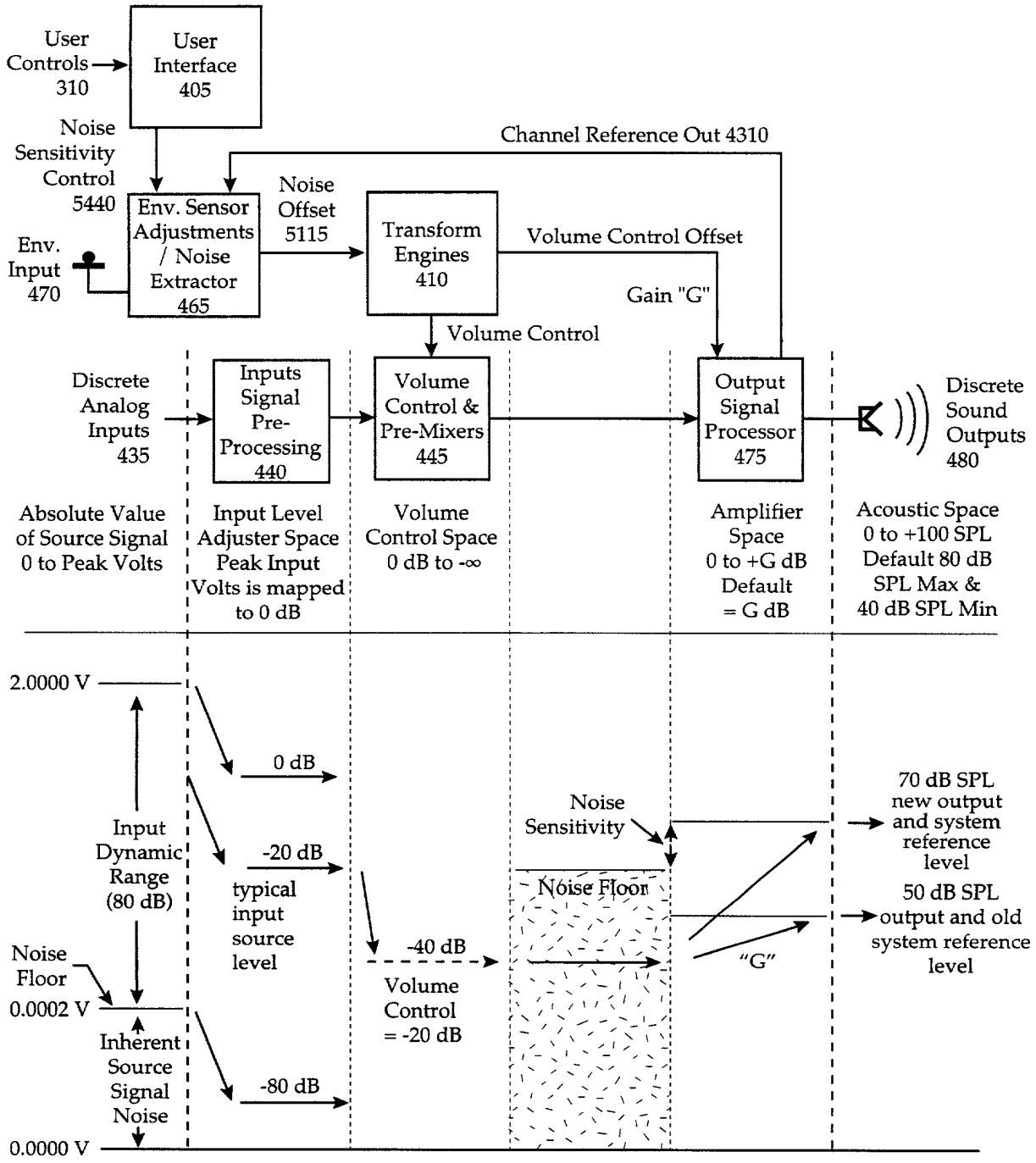

User Controls 310
User Interface 405
Noise Sensitivity Control 5440
Channel Reference Out 4310
Env. Input 470
Env. Sensor Adjustments / Noise Extractor 465
Noise Offset 5115
Transform Engines 410
Volume Control Offset
Gain "G"
Volume Control
Discrete Analog Inputs 435
Inputs Signal Pre-Processing 440
Volume Control & Pre-Mixers 445
Output Signal Processor 475
Discrete Sound Outputs 480
Absolute Value of Source Signal 0 to Peak Volts
Input Level Adjuster Space Peak Input Volts is mapped to 0 dB
Volume Control Space 0 dB to -∞
Amplifier Space 0 to +G dB Default = G dB
Acoustic Space 0 to +100 SPL Default 80 dB SPL Max & 40 dB SPL Min
2.0000 V
0 dB
-20 dB
typical input source level
-40 dB
Volume Control = -20 dB
Noise Sensitivity
Noise Floor
70 dB SPL new output and system reference level
50 dB SPL output and old system reference level
"G"
Input Dynamic Range (80 dB)
Noise Floor
0.0002 V
Inherent Source Signal Noise
-80 dB
0.0000 V

FIG. 76

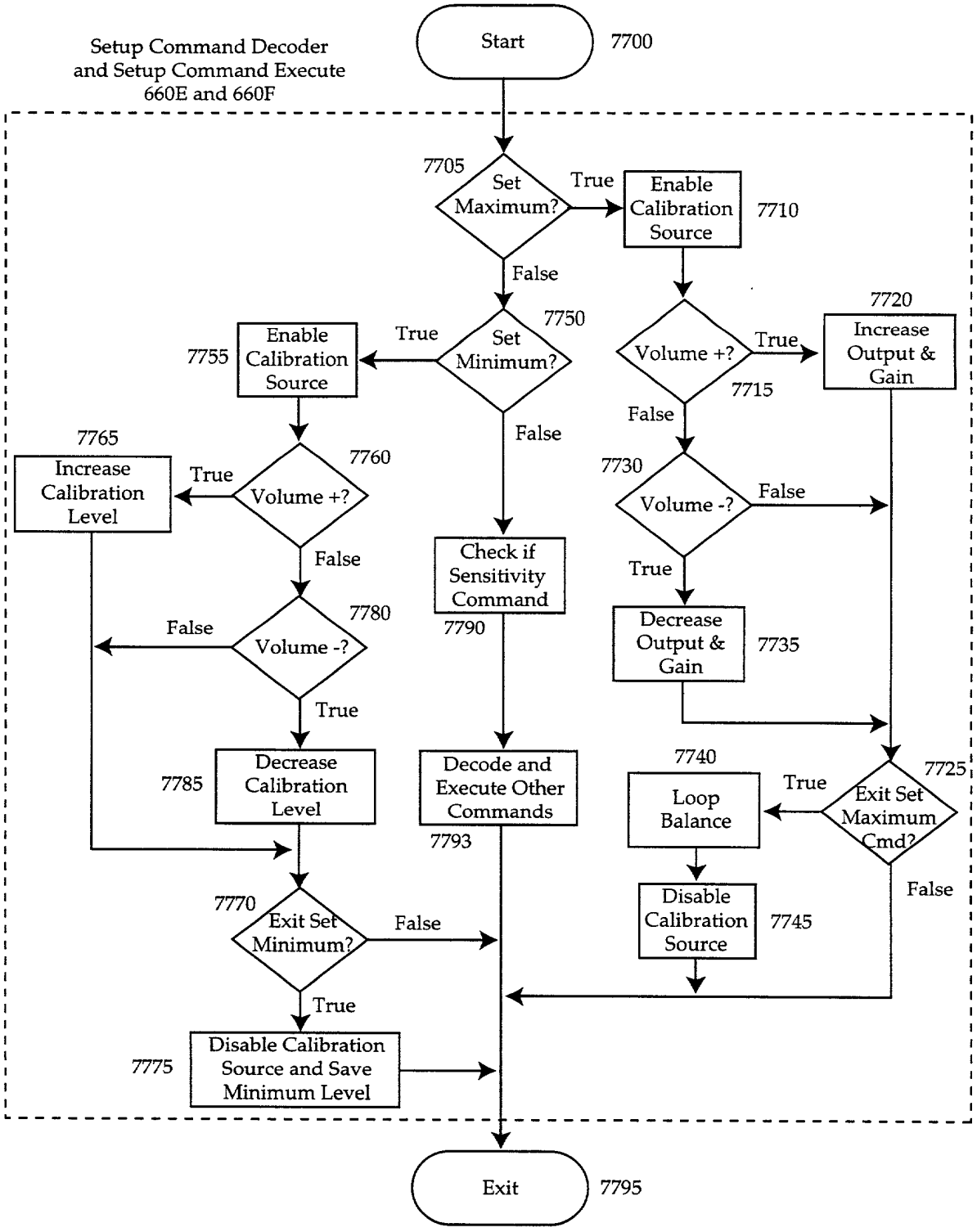

Setup Command Decoder and Setup Command Execute 660E and 660F
Start
7700
7705
Set Maximum?
True
Enable Calibration Source
7710
False
7750
Set Minimum?
True
7755
Enable Calibration Source
False
Check if Sensitivity Command
7790
Decode and Execute Other Commands
7793
7720
Volume +?
True
Increase Output & Gain
7715
False
7730
Volume -?
False
True
Decrease Output & Gain
7735
7765
Increase Calibration Level
True
7760
Volume +?
False
7780
Volume -?
False
True
7785
Decrease Calibration Level
7740
Loop Balance
True
7725
Exit Set Maximum Cmd?
False
Disable Calibration Source
7745
7770
Exit Set Minimum?
False
True
7775
Disable Calibration Source and Save Minimum Level
Exit
7795

FIG. 77

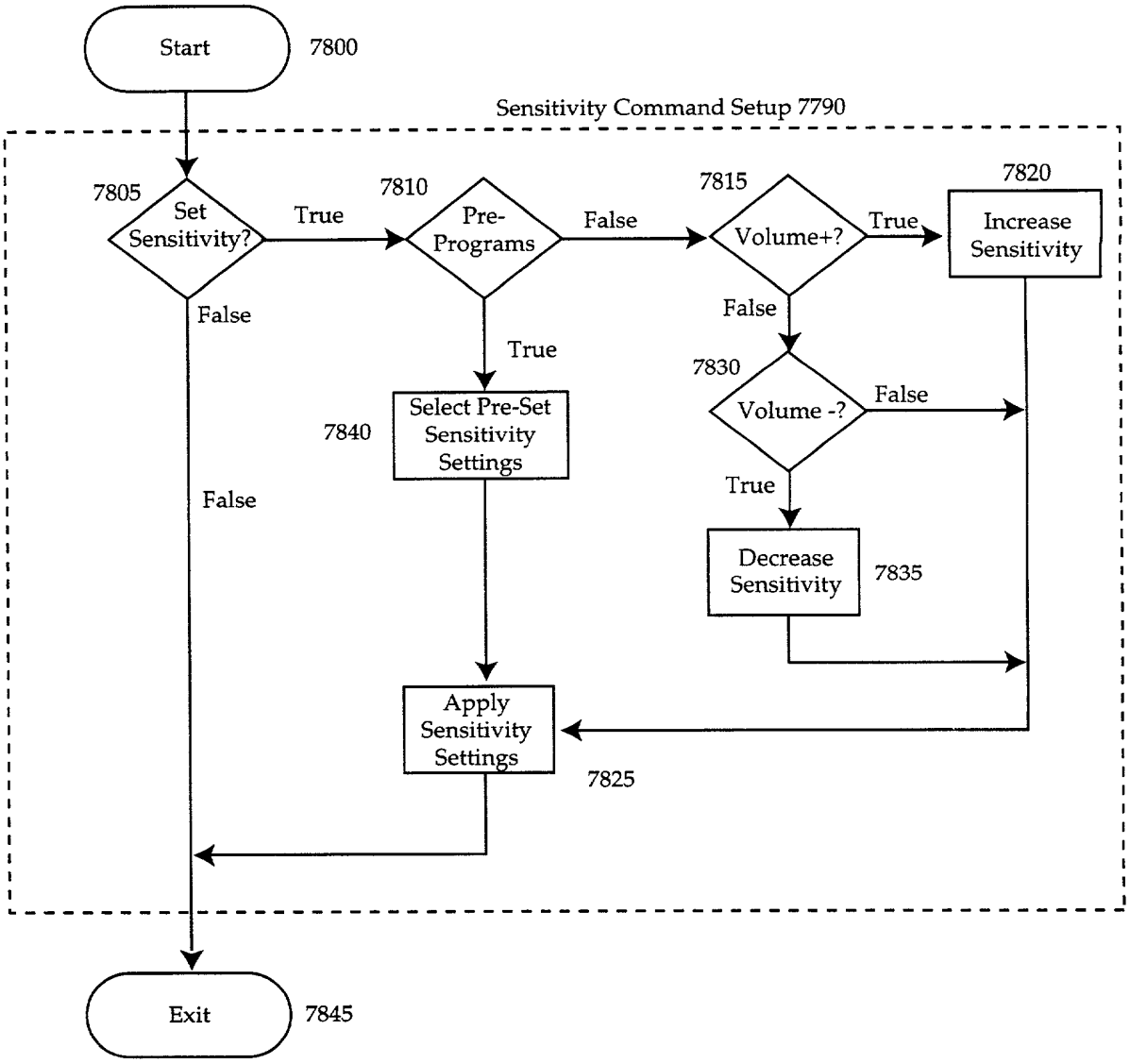

Start
7800
Sensitivity Command Setup 7790
7805
Set Sensitivity?
True
7810
Pre-Programs
False
7815
Volume+?
True
7820
Increase Sensitivity
False
True
False
7830
Volume -?
False
7840
Select Pre-Set Sensitivity Settings
True
Decrease Sensitivity
7835
False
Apply Sensitivity Settings
7825
Exit
7845

FIG. 78

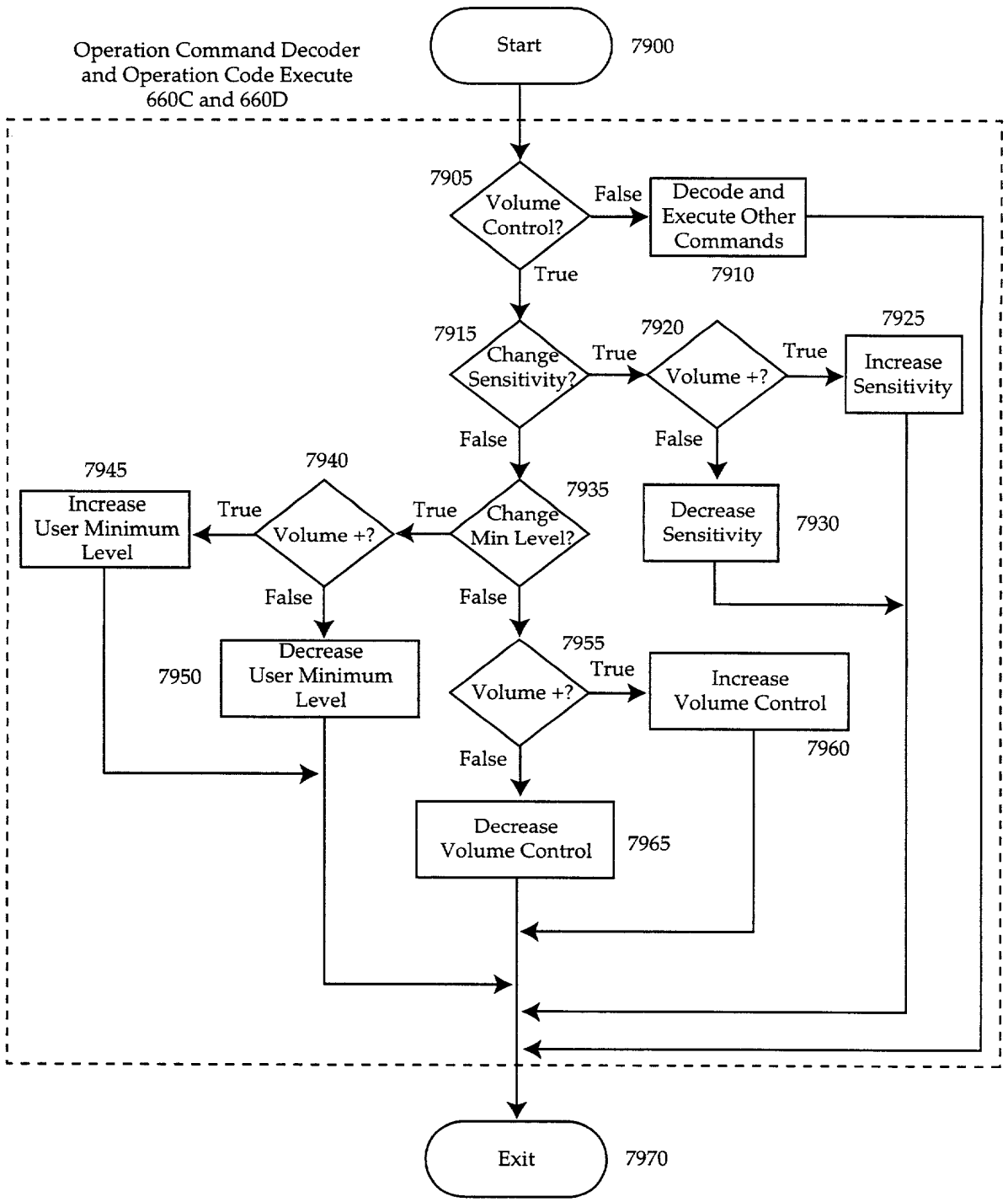

Operation Command Decoder and Operation Code Execute 660C and 660D
Start
7900
7905
Volume Control?
False
Decode and Execute Other Commands
7910
True
7915
Change Sensitivity?
True
7920
Volume +?
True
7925
Increase Sensitivity
False
False
7945
Increase User Minimum Level
True
7940
Volume +?
True
Change Min Level?
7935
Decrease Sensitivity
7930
False
False
7950
Decrease User Minimum Level
7955
Volume +?
True
Increase Volume Control
7960
False
Decrease Volume Control
7965
Exit
7970

FIG. 79